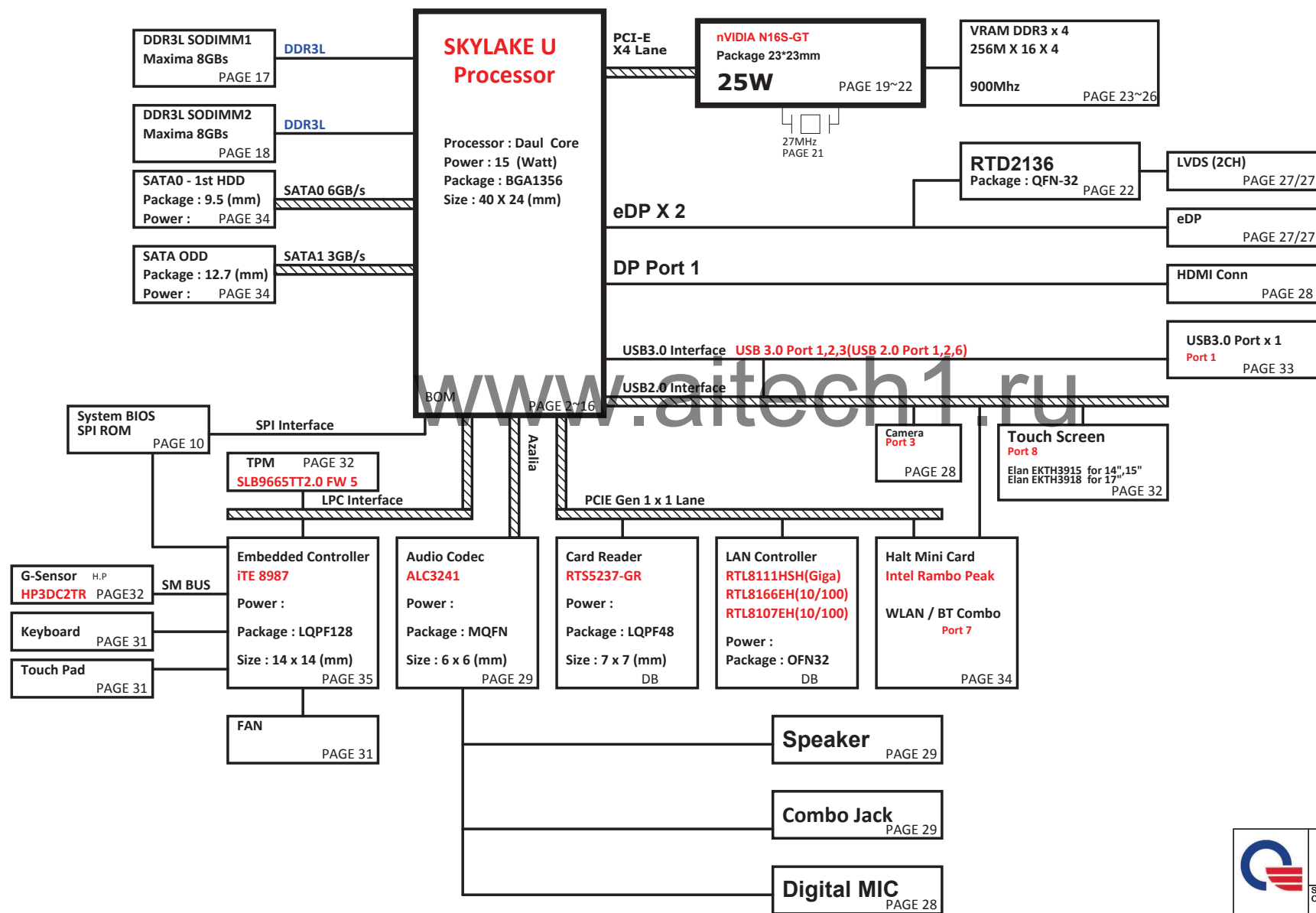


DIS (14" / 15" / 17") Chocolate

Intel SKYLAKE ULT Platform Block Diagram

PCB 6L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : BOT



+3V 4,10,11,12,13,14,15,16,17,18,20,27,28,29,30,31,32,33,34,35,41,43,44
+1.0V 4,6,16,32,35,40
+VCCSTPLL 4,5,6,9,40,41

HDMI

28 IN_D2# IN_D2# E55
28 IN_D2 IN_D2 F55
28 IN_D1# IN_D1# E58
28 IN_D1 IN_D1 F58
28 IN_D0# IN_D0# F53
28 IN_D0 IN_D0 G53
28 IN_D0# IN_D0# G53
28 IN_D0 IN_D0 F56
28 IN_CLK# IN_CLK# G56
28 IN_CLK IN_CLK G56

U16A SKL_ULT ? Need apply PN

DDI1_TXN[0] DDI1_TXP[0]
DDI1_TXN[1] DDI1_TXP[1]
DDI1_TXN[2] DDI1_TXP[2]
DDI1_TXN[3] DDI1_TXP[3]
DDI2_TXN[0] DDI2_TXP[0]
DDI2_TXN[1] DDI2_TXP[1]
DDI2_TXN[2] DDI2_TXP[2]
DDI2_TXN[3] DDI2_TXP[3]

EDP_TXN[0] EDP_TXP[0]
EDP_TXN[1] EDP_TXP[1]
EDP_TXN[2] EDP_TXP[2]
EDP_TXN[3] EDP_TXP[3]
EDP_AUXN EDP_AUXP
EDP_DISP_UTIL

C47 INT_EDP_TXN0
C46 INT_EDP_TXP0
C46 INT_EDP_TXN1
C45 INT_EDP_TXP1
C45 INT_EDP_TXN2
C45 INT_EDP_TXP2
C45 INT_EDP_TXN3
C45 INT_EDP_TXP3

INT_EDP_TXN0 27
INT_EDP_TXP0 27
INT_EDP_TXN1 27
INT_EDP_TXP1 27
INT_EDP_TXN2 27
INT_EDP_TXP2 27
INT_EDP_TXN3 27
INT_EDP_TXP3 27

E45 INT_EDP_AUXN
F45 INT_EDP_AUXP
B52 EDP_DISP_UTIL

INT_EDP_AUXN 27
INT_EDP_AUXP 27
TP46

DDI1_AUXN DDI1_AUXP
DDI2_AUXN DDI2_AUXP
DDI3_AUXN DDI3_AUXP

G50 G50
F50 F50
E48 E48
C48 C48
C46 C46
C46 C46

HDMI_HPD_CON HDMI_HPD_CON 28
ULT_EDP_HPD ULT_EDP_HPD 27,28

GPP_E13/DDPB_HPD0
GPP_E14/DDPC_HPD1
GPP_E15/DDPD_HPD2
GPP_E16/DDPE_HPD3
GPP_E17/EDP_HPD

R12 PCH_LVDS_BLON
R11 PCH_DPST_PWM
U13 PCH_DISP_ON

PCH_LVDS_BLON 28
PCH_DPST_PWM 28
PCH_DISP_ON 28

EDP_BKLTEN EDP_BKLTCTL
EDP_VDDEN

EDP_RCAMP

EDP_RCAMP

*SKL_ULT
REV = 1
1 OF 20

1223 Del R93, R102

1225 DDPC_CTRLDATA
and DDPC_CTRLDATA
reserve TP

eDP_COMPIO and ICOMPO signals should be shorted near
balls and routed with typical impedance <25 mohms

1218 change R96 connection from +1.0V to +VCCIO

0305
Del tp45

35,36,41 H_PROCHOT# R369 49.9/F 4

35 PM_THRMTRIP#

16 XDP_BPM0
16 XDP_BPM1

33 3D_FW_GPIO

R549 0.4 3D_FW_GPIO_R

TP38 CPU_GP1
TP102 CPU_GP2
TP100 CPU_GP3

R191 49.9/F 4
R186 49.9/F 4
R107 49.9/F 4
R101 49.9/F 4

PROC_POPIRCOMP
PCH_OPIRCOMP
OPCE_RCOMP
OPC_RCOMP

AT16
A16
B45
AY5

AT16
A16
B45
AY5

AT16
A16
B45
AY5

AT16
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AY5

U16D SKL_ULT ? Need apply PN

CATERR#
EC_PECI
PROCHOT#
PM_THRMTRIP#
SKTQCC#

CATERR#
EC_PECI
PROCHOT#
PM_THRMTRIP#
SKTQCC#

CATERR#
EC_PECI
PROCHOT#
PM_THRMTRIP#
SKTQCC#

CATERR#
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SKTQCC#

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SKTQCC#

CATERR#
EC_PECI
PROCHOT#
PM_THRMTRIP#
SKTQCC#

CATERR#
EC_PECI
PROCHOT#
PM_THRMTRIP#
SKTQCC#

*SKL_ULT
REV = 1
4 OF 20

+VCCSTPLL
R393 49.9/F 4
1223 change R393 unmount

+1.0V
R74 0.4

R377 51.4 JTAGX_PCH

R378 51.4 JTAG_TMS_PCH

R395 51.4 JTAG_TDI_PCH

R396 51.4 JTAG_TDO_PCH

R379 51.4 JTAG_TCK_PCH

Close to Chipset

0114
Del TP39, Add R549 with 0ohm
mount for 3D camera

Close to EC

PM_THRMTRIP# R392 1K 4

+VCCSTPLL

Processor pull-up (CPU)

TO BE REPLACED WITH 1K OHMS FOR SKL

470 OHM IS FOR I/P

PLACE NEAR CPU

XDP_TMS_CPU R380 51.4

XDP_TDI_CPU R376 51.4

XDP_TDO_CPU R367 51.4

1218 Unmount R380, R367

H_PROCHOT# R44 1K 4

XDP_TCK0 R394 51.4

XDP_TRST#_CPU R372 51.4

+1.0V

R44 1K 4

R394 51.4

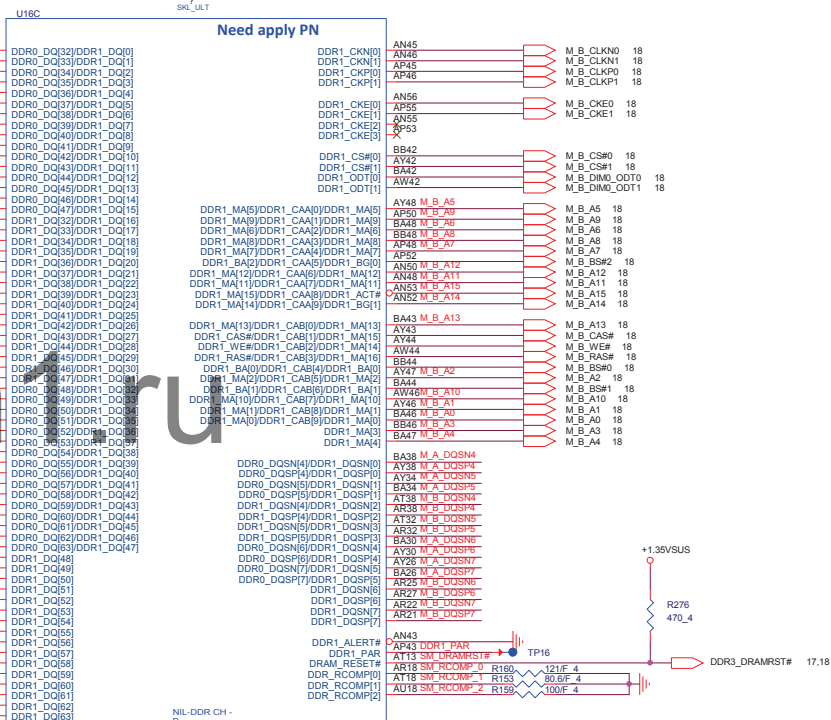
R372 51.4

+1.0V

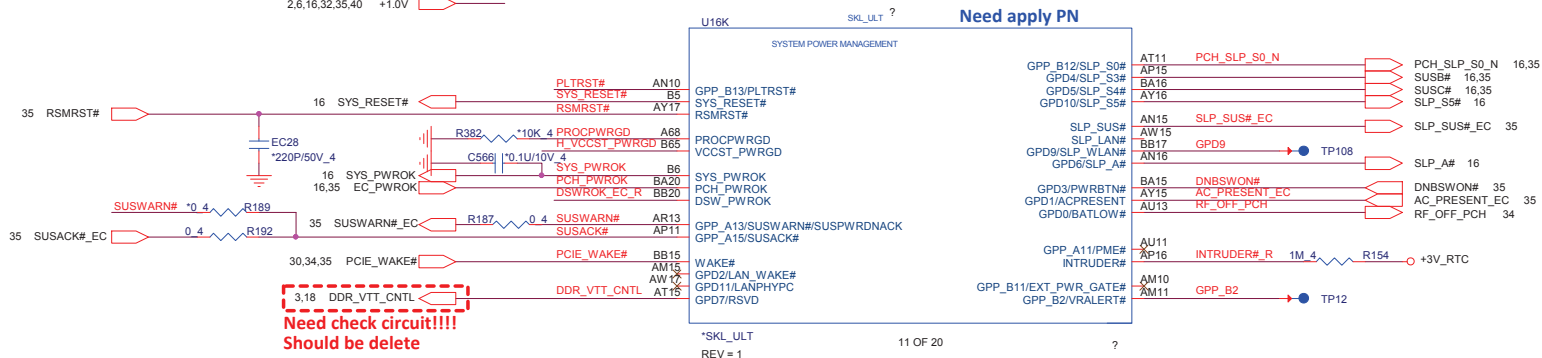
R44 1K 4

R394 51.4

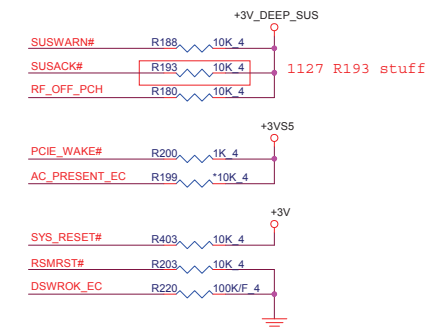
R372 51.4



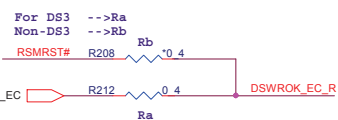
10,11,12,14,15,16,18 +3V_DEEP_SUS
2,10,11,12,13,14,15,16,17,18,20,27,28,29,30,31,32,33,34,35,41,43,44 +3V
10,15,16,32,34,35,37,39,40,43,46 +3VS5
2,5,6,9,40,41 +VCCSTPLL
2,6,16,32,35,40 +1.0V



PCH Pull-high/low(CLG)



For DS3 Sequence

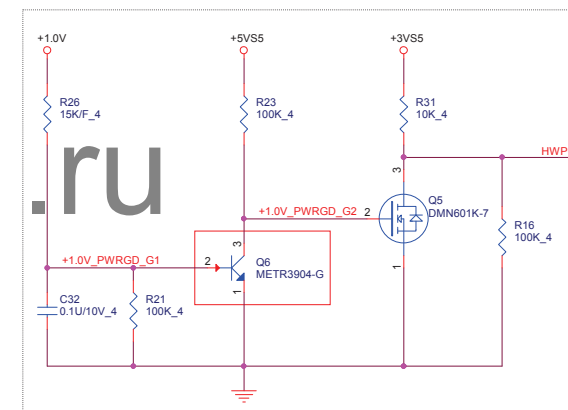
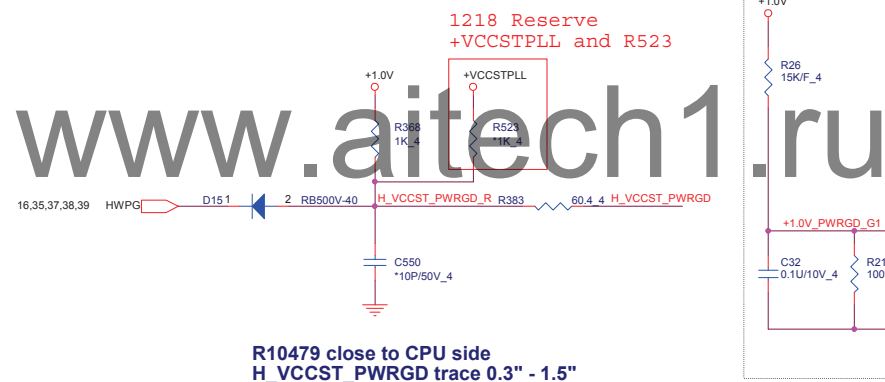
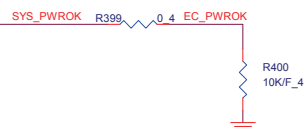


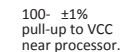
PLTRST#(CLG)

Check Q2010 Rise/Fall time less than 100ns



System PWR_OK(CLG)






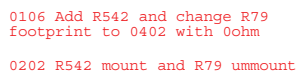
www.aitech1.ru

CLOSE TO CPU
PLACE THE PWR RES.

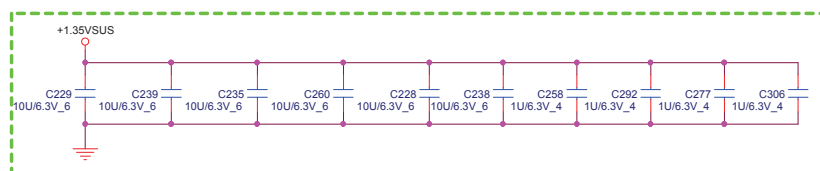
H.O.



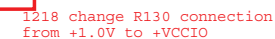
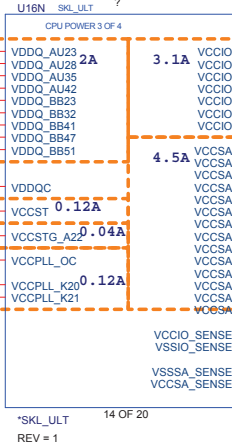
	PROJECT :Y11X-6L Quanta Computer Inc.		
	Size Custom	Document Number 05 -- SKYPAKE 6/20 (POWER-1)	Rev 1A
	Date: Wednesday, May 06, 2015	Sheet 5 of 49	



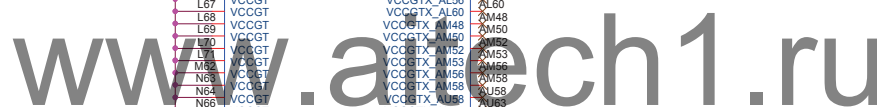
0420 Add R574 NI for Modern Stand by
0428 Add R575 NI for Modern Stand by




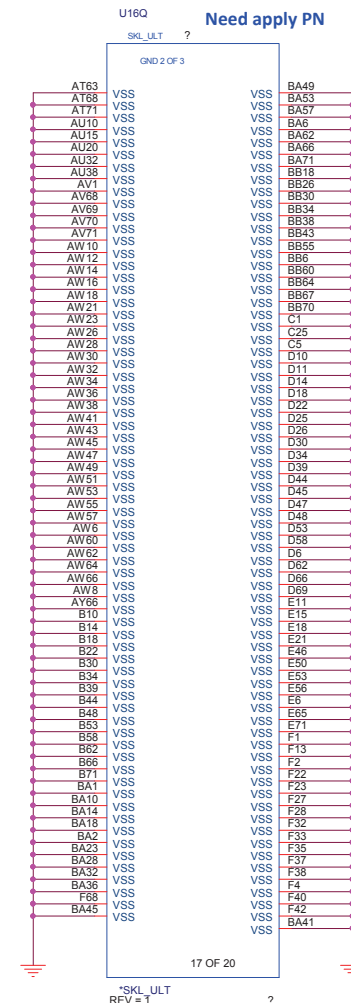
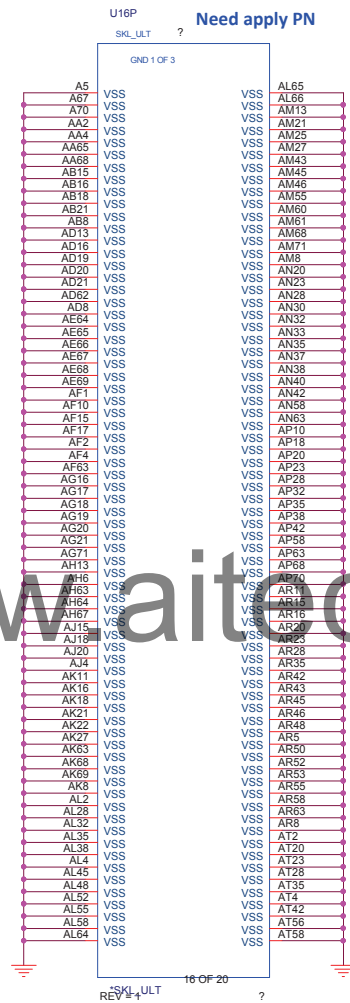
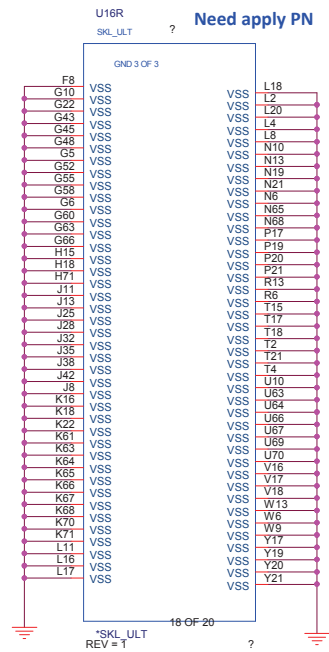
Close to CPU



Power Rail	Description	Control
V _{CC}	Processor IA Cores Power Rail	SVID
V _{CCGT}	Processor Graphics Power Rails	SVID
V _{CCGTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V _{CCSA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
V _{CCIO}	IO Power Rail	Fixed
V _{CCST}	Sustain Power Rail	Fixed
V _{CCPLL}	Processor PLLs power rail	Fixed
V _{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V _{CCOPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCOPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCEOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

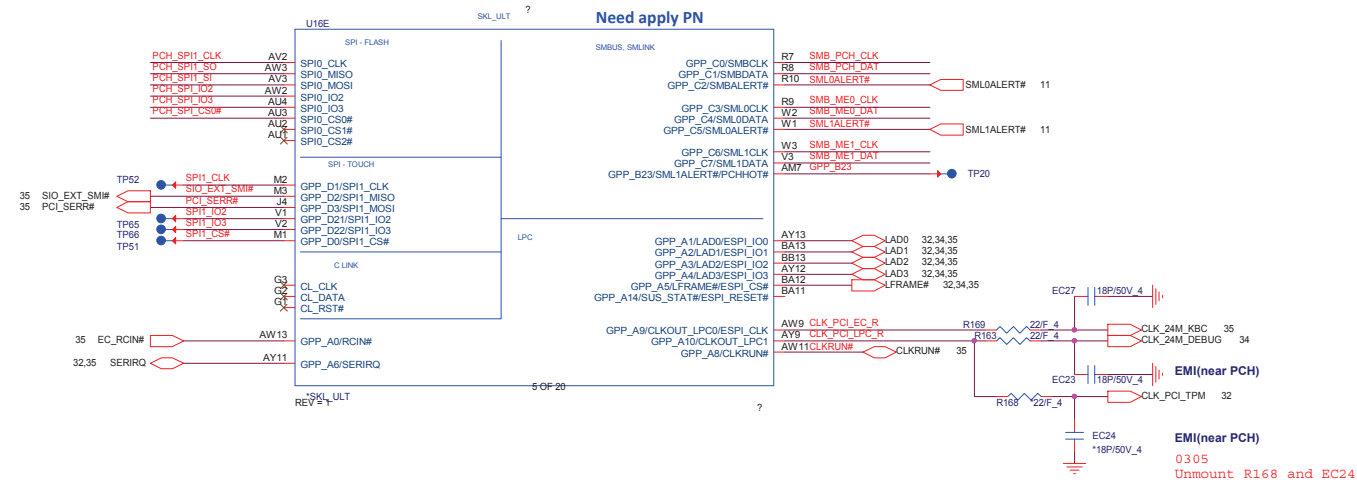


	PROJECT :Y11X-6L Quantia Computer Inc.		
	Size Custom	Document Number 07 -- SKYPAKE 8/20 (POWER-3)	Rev 1A
	Date: Wednesday, May 06, 2015	Sheet 7 of 49	

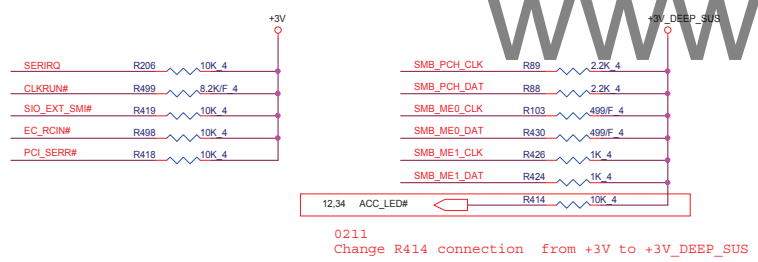




+3V_DEEP_SUS 4,11,12,14,15,16,18
+3V 2,4,11,12,13,14,15,16,17,18,20,27,28,29,30,31,32,33,34,35,41,43,44
+5V 28,29,30,31,32,33,34,43
+1.0V 2,4,6,16,32,35,40
+3VSS 4,15,16,32,34,35,37,39,40,43,46



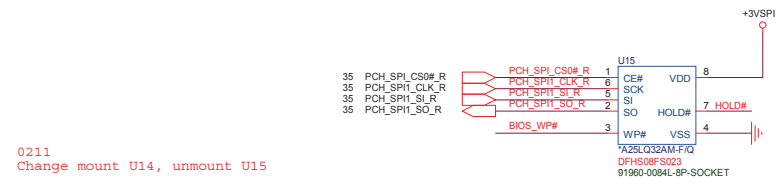
GPIO Pull UP



PCH SPI ROM(CLG)

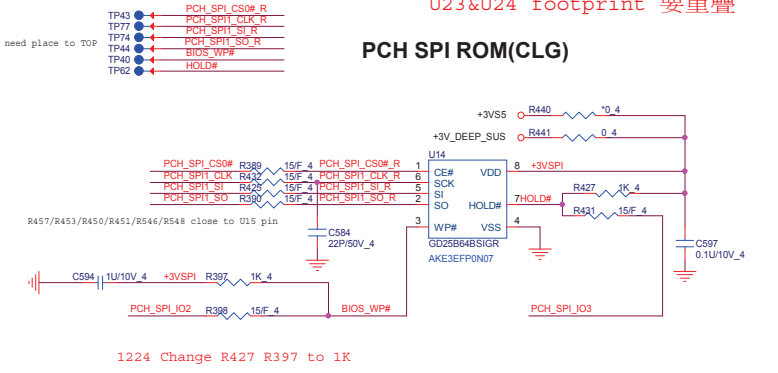
Vender	Size	P/N
EQN	8MB	AKE3EZN0Q01 (EN25QH64-104HiP)
Winbond	8MB	AKE3EFP0N07 (W25Q64FVSSIQ)
GigaDevice	8MB	AKE3EGN0Q01 (GD25B64BSIGR)
Socket		DFHS08FS023

4M SPI ROM Socket

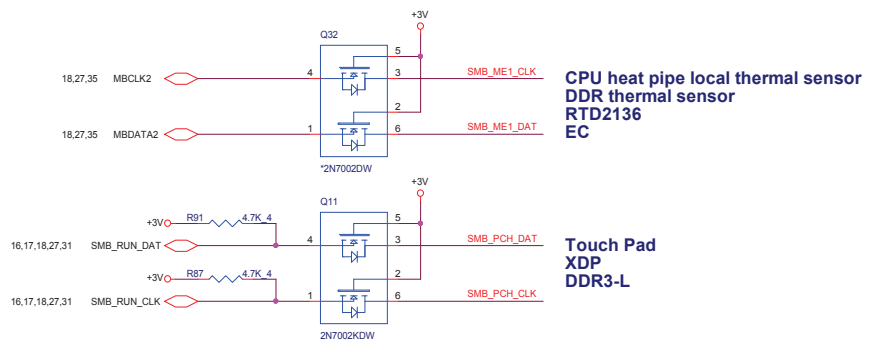


U23&U24 footprint 要重叠

PCH SPI ROM(CLG)

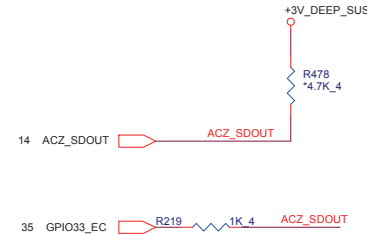
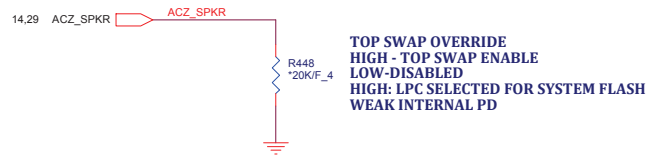


SMBus/Pull-up(CLG)



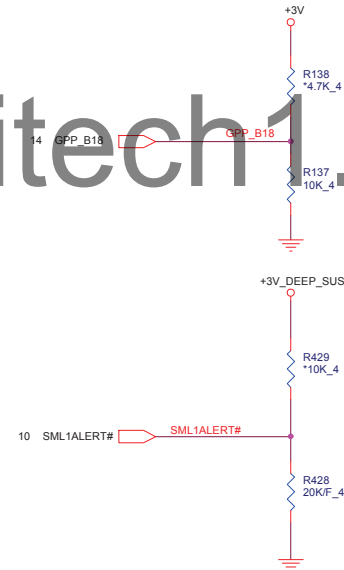
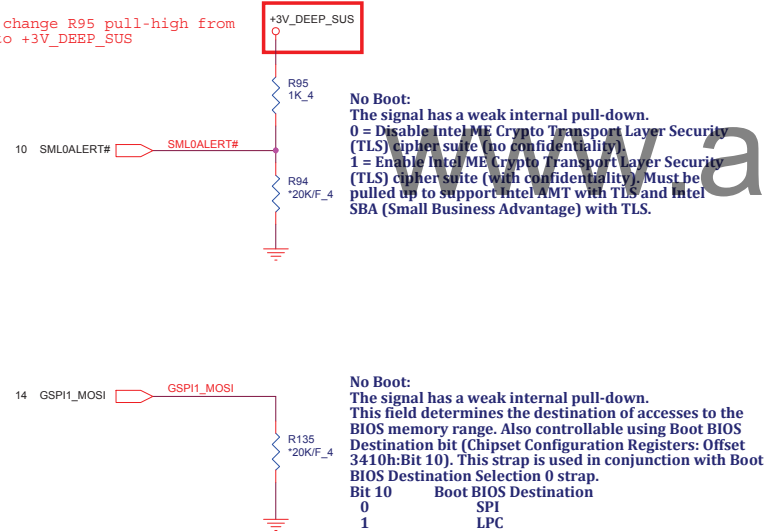
Functional Strap Definitions

DESIGN NOTE:
WEAK PULL UP RESISTOR PRESENT ON THIS NET



No Boot:
The signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. This function is useful when running ITP/XDP.

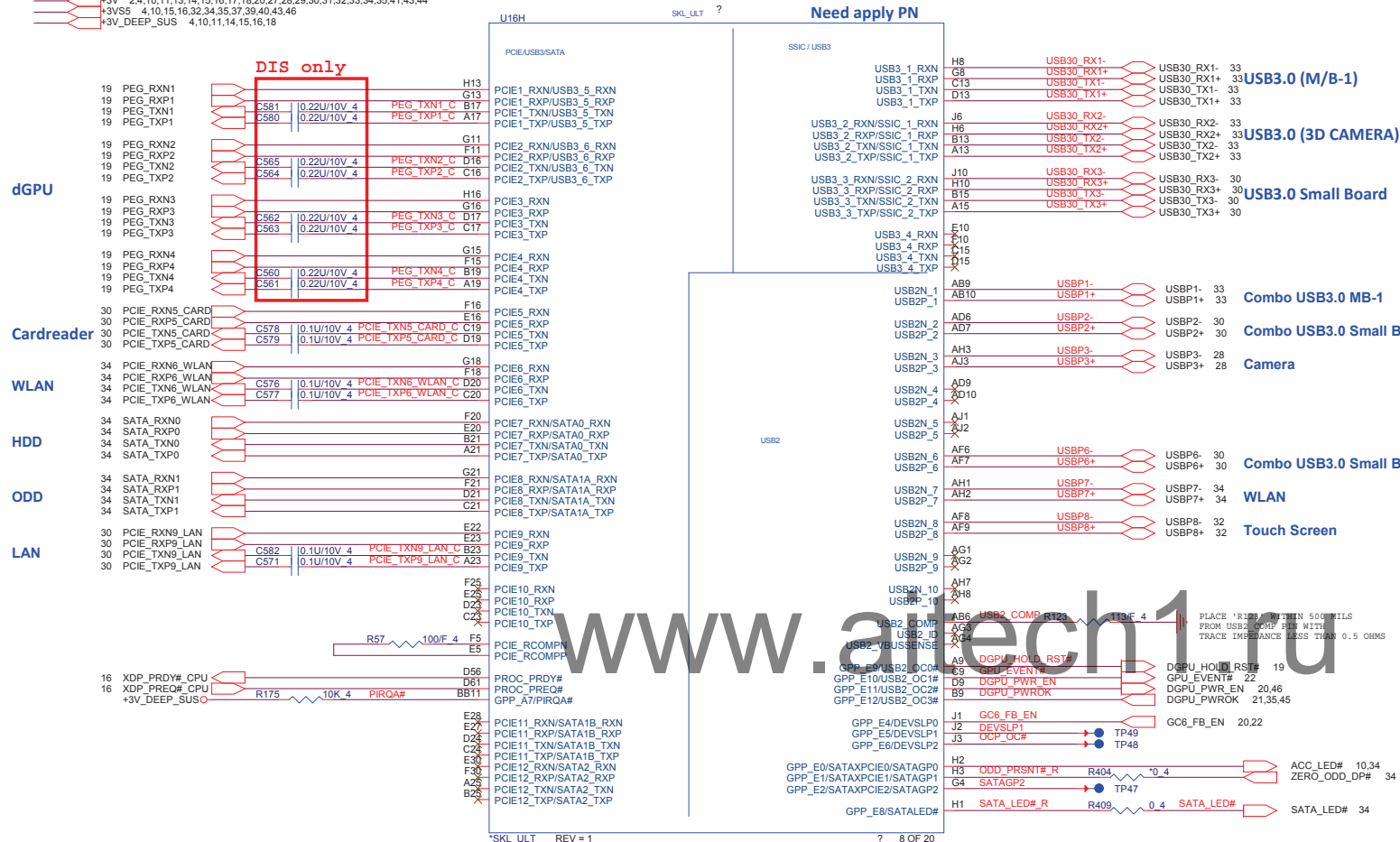
1212 change R95 pull-high from +3V to +3V_DEEP_SUS



No Boot:
The signal has a weak internal pull-down.
0 = Disable No Reboot mode.
1 = Enable No Reboot mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

No Boot:
The signal has a weak internal pull-down.
0 = LPC Is selected for EC.
1 = eSPI Is selected for EC.

+3V 2,4,10,11,13,14,15,16,17,18,20,27,28,29,30,31,32,33,34,35,41,43,44
 +3VSS 4,10,15,16,32,34,35,37,39,40,43,46
 +3V_DEEP_SUS 4,10,11,14,15,16,18



PCI-E Port Mapping Table

PCI-E Port	Function	CLK RQ Port	Function
Port1	dGPU	Port0	Un-used
Port2	dGPU	Port1	CardReader
Port3	dGPU	Port2	WLAN
Port4	dGPU	Port3	LAN
Port5	CardReader	Port4	VGA
Port6	WLAN	Port5	Un-used
Port7	HDD		
Port8	ODD		
Port9	LAN		
Port10	Un-used		

USB3.0 Port Mapping Table

USB3.0	Function
PORT-1	USB3.0 MB-1
PORT-2	NC
PORT-3	Cobime USB3.0 Smaii Board
PORT-4	NC

USB2.0 Port Mapping Table

USB2.0	Function
PORT-1	Cobime USB3.0 MB-1
PORT-2	Cobime USB3.0 Smaii Board
PORT-3	Camera
PORT-4	NC
PORT-5	NC
PORT-6	Cobime USB3.0 Smaii Board
PORT-7	WLAN
PORT-8	Touch Screen
PORT-9	NC
PORT-10	NC

+3V_RTC 4,15,32
 +1.0V_DEEP_SUS 9,15,39
 +3V 2,4,10,11,12,14,15,16,17,18,20,27,28,29,30,31,32,33,34,35,41,43,44

0225 Change VGA CLK from Port4 to Port0

VGA

Cardreader

WLAN

LAN

PCIE_CLKREQ4#

PCIE_CLKREQ5#

PCIE_CLKREQ6#

PCIE_CLKREQ7#

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PCIE_CLKREQ212#

PCIE_CLKREQ213#

PCIE_CLKREQ214#

PCIE_CLKREQ215#

PCIE_CLKREQ216#

PCIE_CLKREQ217#

PCIE_CLKREQ218#

PCIE_CLKREQ219#

PCIE_CLKREQ220#

PCIE_CLKREQ221#

PCIE_CLKREQ222#

PCIE_CLKREQ223#

PCIE_CLKREQ224#

PCIE_CLKREQ225#

PCIE_CLKREQ226#

PCIE_CLKREQ227#

PCIE_CLKREQ228#

PCIE_CLKREQ229#

PCIE_CLKREQ230#

PCIE_CLKREQ231#

PCIE_CLKREQ232#

PCIE_CLKREQ233#

PCIE_CLKREQ234#

PCIE_CLKREQ235#

PCIE_CLKREQ236#

PCIE_CLKREQ237#

PCIE_CLKREQ238#

PCIE_CLKREQ239#

PCIE_CLKREQ240#

PCIE_CLKREQ241#

PCIE_CLKREQ242#

PCIE_CLKREQ243#

PCIE_CLKREQ244#

PCIE_CLKREQ245#

PCIE_CLKREQ246#

PCIE_CLKREQ247#

PCIE_CLKREQ248#

PCIE_CLKREQ249#

PCIE_CLKREQ250#

PCIE_CLKREQ251#

PCIE_CLKREQ252#

PCIE_CLKREQ253#

PCIE_CLKREQ254#

PCIE_CLKREQ255#

PCIE_CLKREQ256#

PCIE_CLKREQ257#

PCIE_CLKREQ258#

PCIE_CLKREQ259#

PCIE_CLKREQ260#

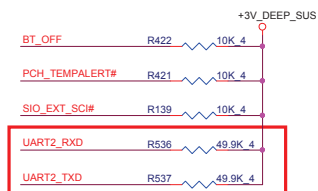
PCIE_CLKREQ261#

PCIE_CLKREQ262#

PCIE_CLKREQ263#

Skylake (GPIO)

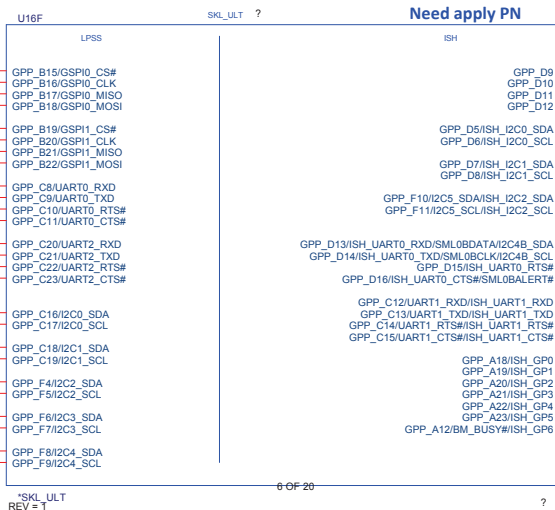
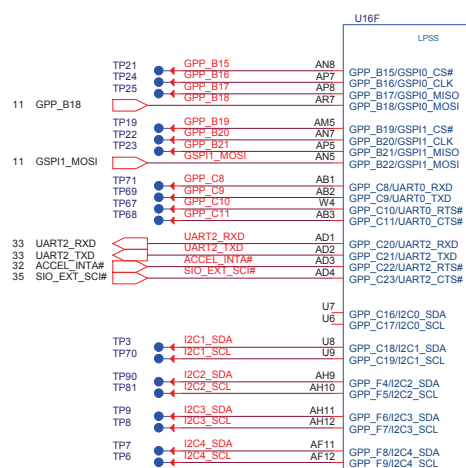
+3V 2,4,10,11,12,13,15,16,17,18,20,27,28,29,30,31,32,33,34,35,41,43,44
+3V_DEEP_SUS 4,10,11,12,15,16,18



1227 Add R536 and R537 for
UART2 function reserved



1223 Add R525

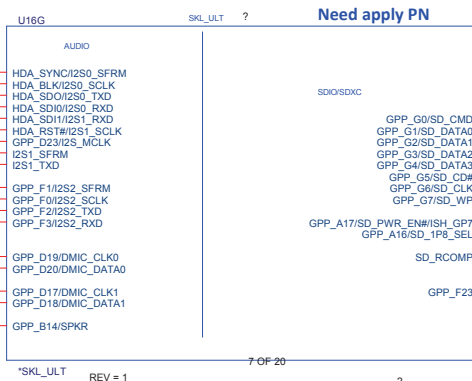
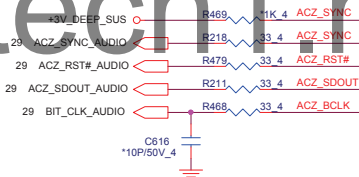


0224
Unmount R547
0114
Del TP57, Add R547 with 0ohm

0305
Del TP73

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HDA Bus(CLG)



0129
Del TP110 add GPP_A16

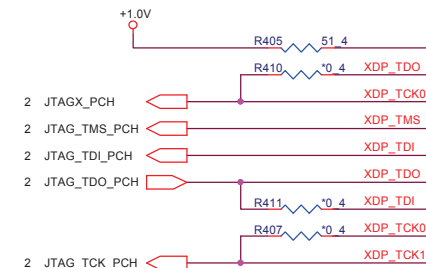
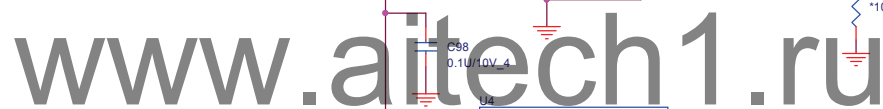
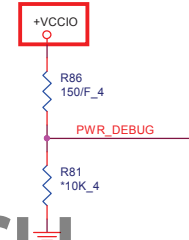
Skylake U	BOARD_ID[8:7]	BOARD_ID[6:5]	Board ID [4:3]	BOARD_ID[2:1]	BOARD_ID0
Model	ID8 ID7	ID6 ID5	ID4 ID3	ID2 ID1	ID0
Definition	Reserve (Default = 00)	Reserve (Default = 00)	00 Single Rank (X1B) 01 Dual Rank (X1B) 10 Meso-AMD (X1A) 11 Reserve	00 14" 01 15" 10 17" 11 Reserve	0 : UMA 1 : DIS



PROJECT :Y11X-6L
Quanta Computer Inc.

Size Custom Document Number 14 -- SKYPAKE 19/20 (GPIO) Rev 1A
Date: Wednesday, May 06, 2015 Sheet 14 of 49






```
1230 Change C587
size to 0603
```

$$\text{PEX IOVDD} + \text{PEX IOVDDQ} = 1.042\text{A}$$

PEX_PLL_HVDD +
PEX_SVDD 3V3 = 143mA

NVDD = 32.22 ~ 26.66 A +VGACORE

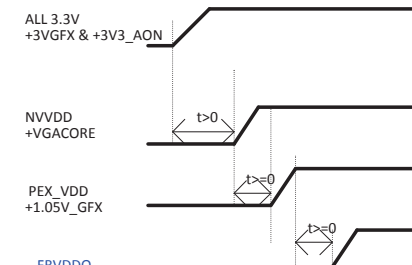
VDD33 = 56mA

C243 4.7U/6.3V_6 Near GPU

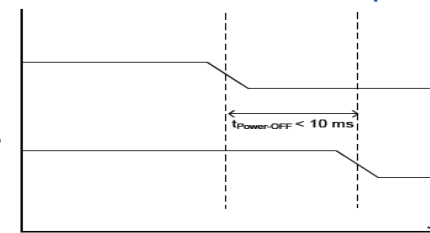
1230 Change C247,
C294 size to 0402

Power up sequence

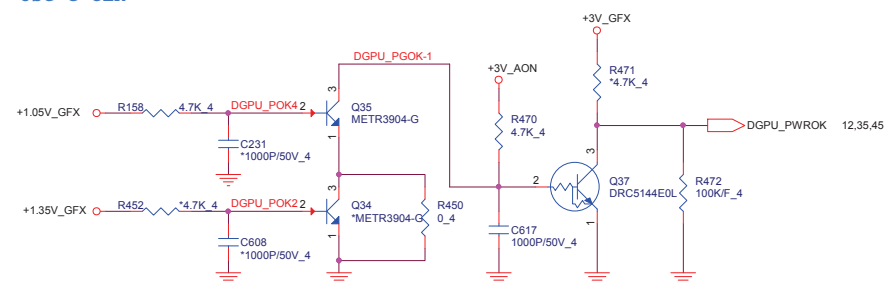
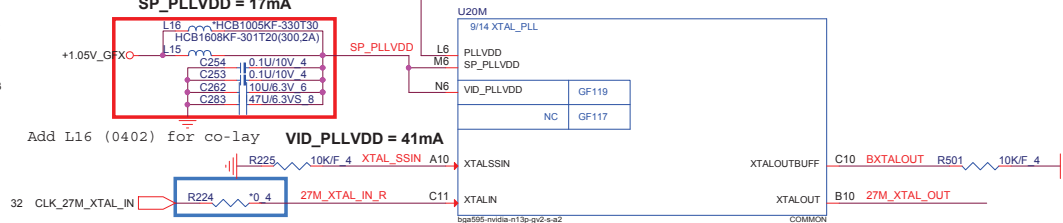
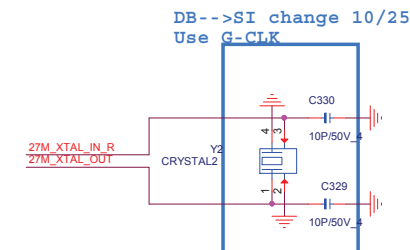
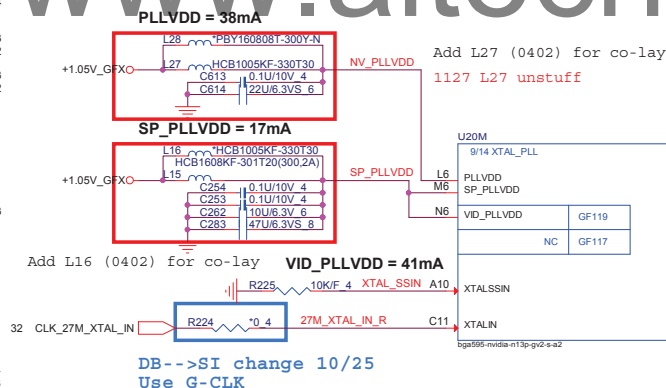
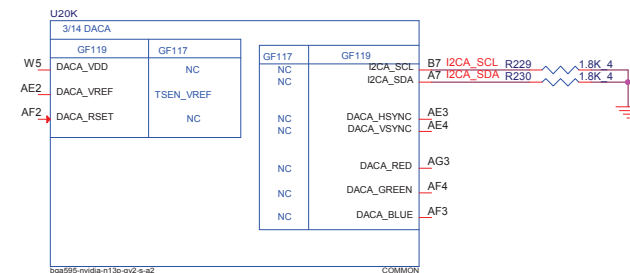
Power down sequence

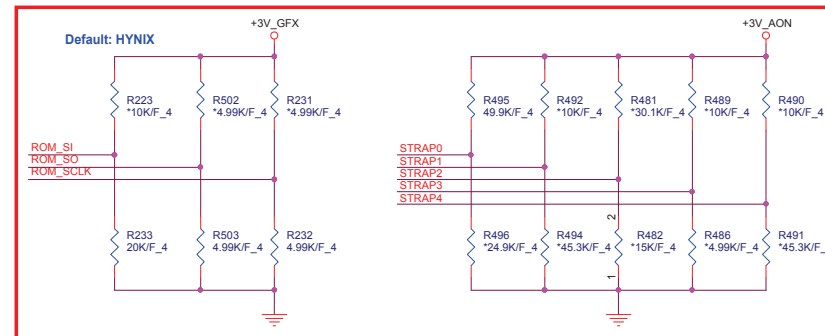


Last Rail to Power

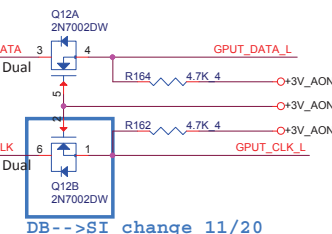








Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111



VRAM Configuration Table							
RAMCFG [3:0]		DESCRIPTION	Vendor	Vendor P/N	Strapping	TOP B/S	QBC
0000		DDR3L 256Mx16, 64bit, 4Gb,900MHz	HYNIX	H5TC4G63CFR-N0C	0x2	AKD5PZDTW01	AKD5PZDTW02
0010		DDR3L 256Mx16, 64bit, 4Gb,900MHz	Micron	MT41J256M16BA-093G:E	0x2	AKD5PZSTL00	AKD5PZSTL01
0001		DDR3L 256Mx16, 64bit, 4Gb,900MHz	SAMSUNG	K4W4G1646E-BC1A	0x1	AKD5PGDT500	AKD5PGDT501

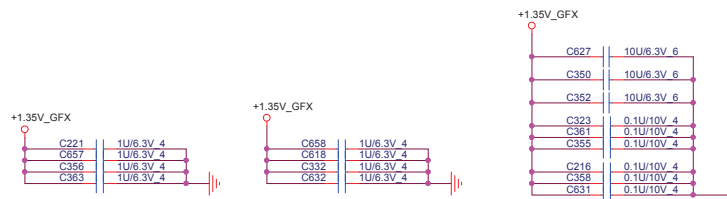
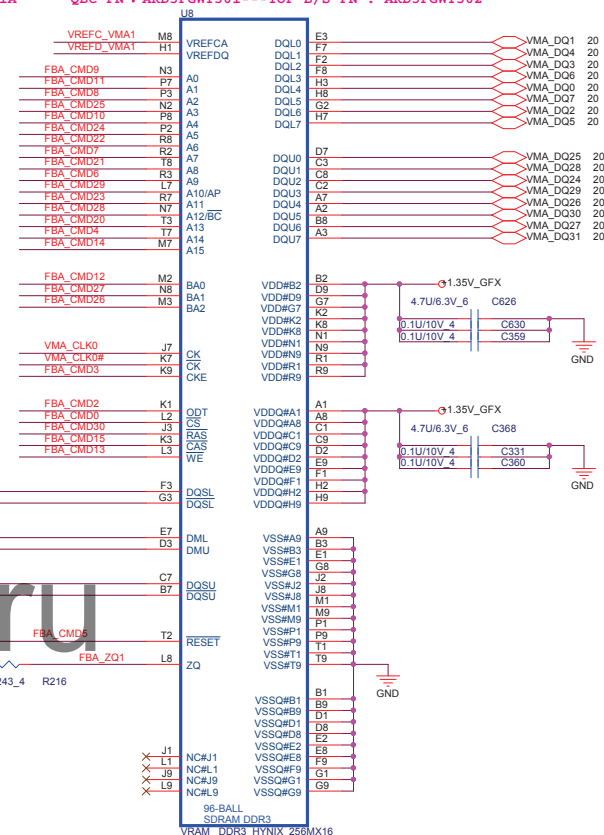
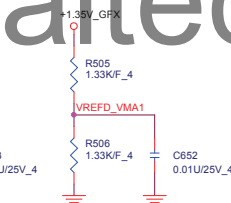


GPIO	I/O	PIN	USAGE
0	IN	FB_CLAMP_MON	FB Clamp monitor
1	OUT	MEM_VDD_CTL	Memory VDD VID
2	OUT	LCD_BL_PWM	Panel Backlight PWM
3	OUT	LCD_VCC	PANEL POWER ENABLE
4	OUT	LCD_BLEN	PANEL BACKLIGHT ENABLE
5	OUT	Reserved	--
6	OUT	FB_CLAMP_TGL_REQ	Active low FB Clamp toggle request
7	OUT	3D_VISION	3D VISION LEFT/RIGHT signal
8	I/O	OVERT	ACTIVE LOW THERMAL OVER TEMP
9	I/O	ALERT	ACTIVE LOW THERMAL ALERT
10	OUT	MEM_VREF_CTL	MEMMORY VREF CONTROL
11	OUT	PWR_VID	GPU CORE_VDD PWM Control signal
12	IN	PWR_LEVEL	AC Power detect or power supply overdraw input
13	OUT	PSI	Phase Shedding




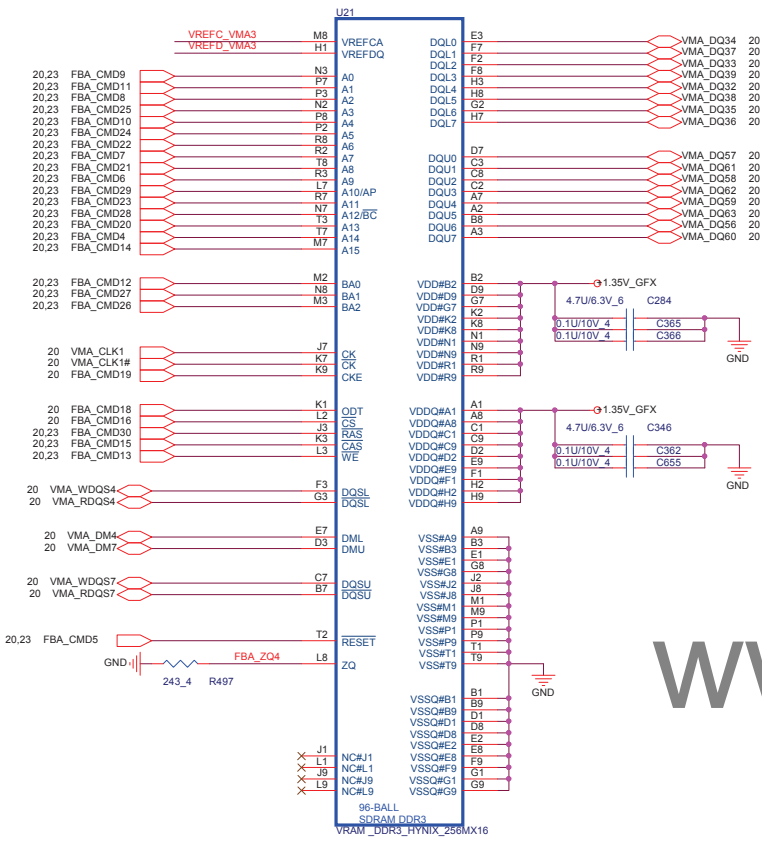
PROJECT :Y11X-6L
Quanta Computer Inc.

Size Custom	Document Number 22 – N15S-GT (GPIO/STRAPS)	Rev 1A
Date: Wednesday, May 06, 2015		Sheet 22 of 49

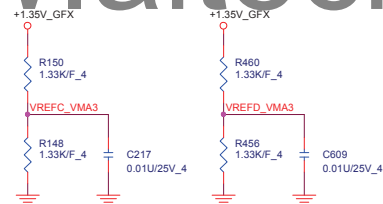
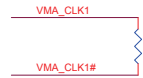


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		PROJECT :Y11X-6L Quanta Computer Inc.	
Size Custom	Document Number 24 -- Reserve		Rev 1A
Date: Wednesday, May 06, 2015		Sheet 24 of 49	

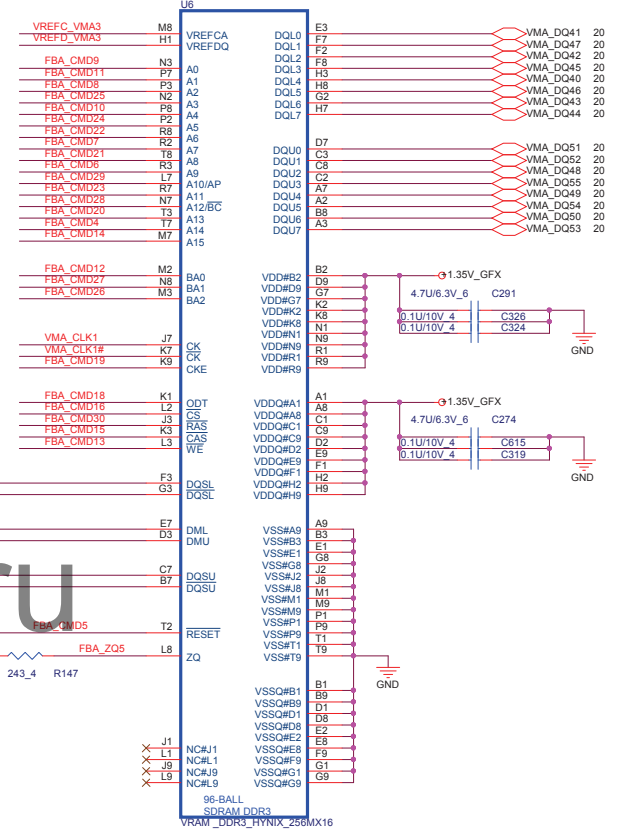


162_1% ohm CS11622FB07 RES CHIP 162 1/16W +-1%(0402)
CS11622FB15 RES CHIP 162 1/16W +-1%(0402)

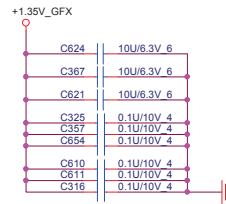
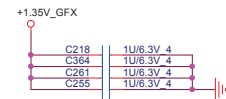
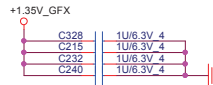
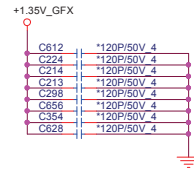


HYU 256Mx16, H5TC4G63AFR-11C
MIC 256Mx16, MT41J256M16HA-093G:E
SAM 256Mx16, K4W4G1646D-BC1A

QBC PN : AKD5PGWTW08---TOP B/S PN : AKD5PGWTW07
QBC PN : AKD5PZSTL01---TOP B/S PN : AKD5PZSTL00
QBC PN : AKD5PGWT501---TOP B/S PN : AKD5PGWT502




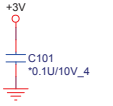
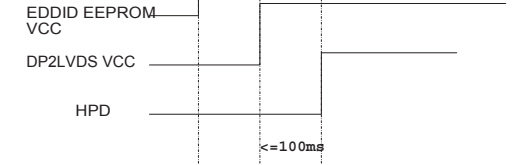
FOR EMI Request



PROJECT :Y11X-6L
Quanta Computer Inc.

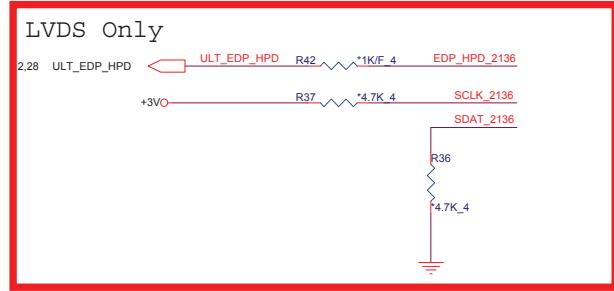
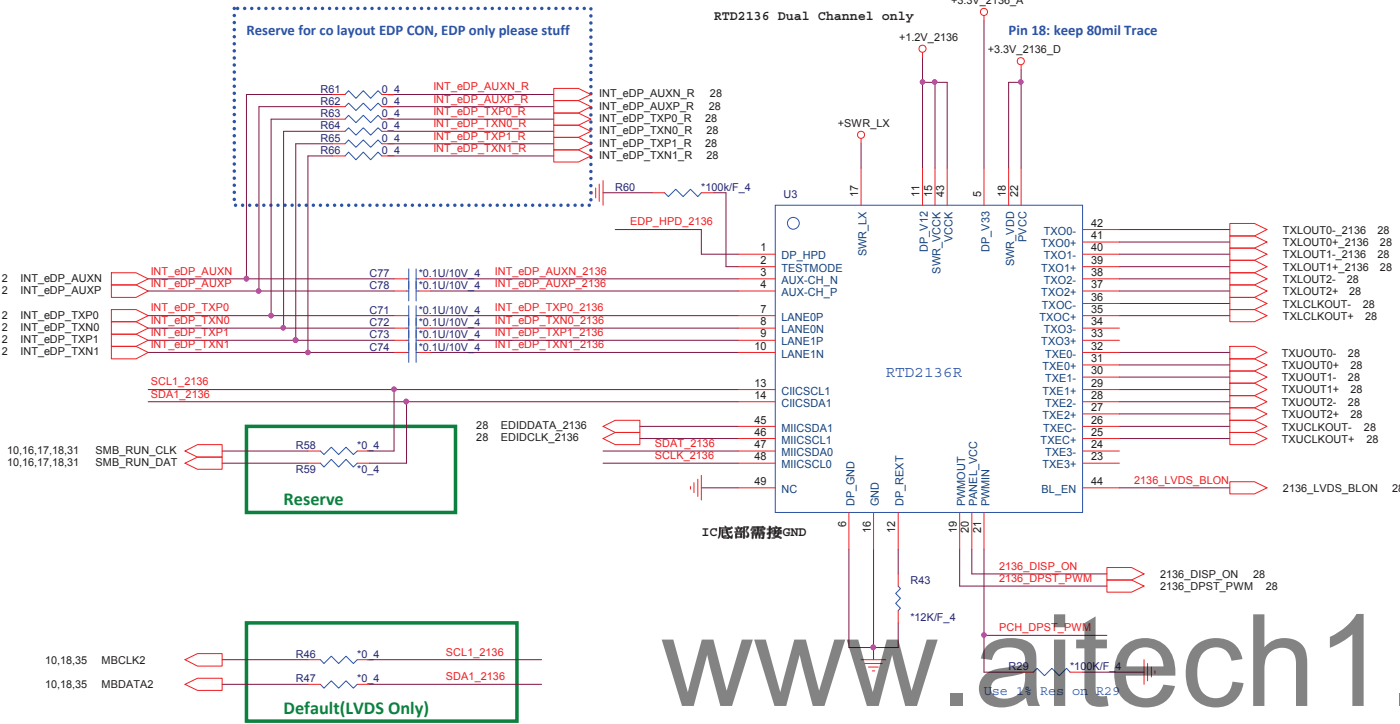
www.aitech1.ru

		PROJECT :Y11X-6L Quanta Computer Inc.	
Size Custom	Document Number 26 -- Reserve		Rev 1A
Date: Wednesday, May 06, 2015 Sheet 26 of 49			



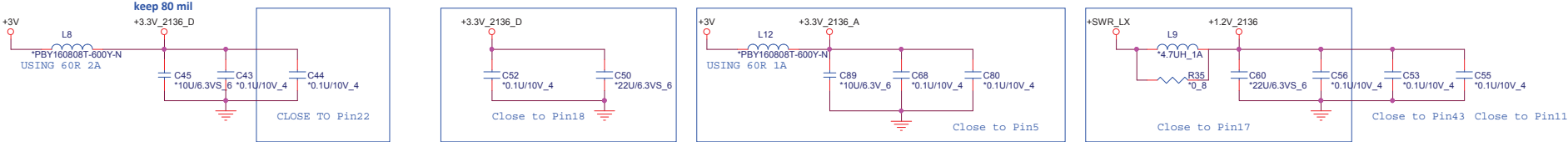
www.aitech1.ru

For eDP, close to U3



24,10,11,12,13,14,15,16,17,18,20,28,29,30,31,32,33,34,35,41,43,44 +3V

L9: need use CV-4709MN00 for Vendor suggestion



SWR MODE	LDO MODE
Stuff L9	Stuff R35

PROJECT :Y11X-6L
Quanta Computer Inc.

Size Custom

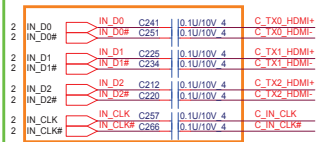
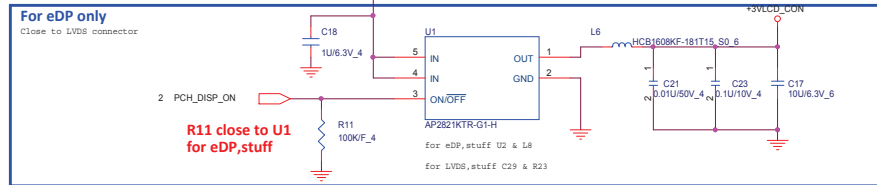
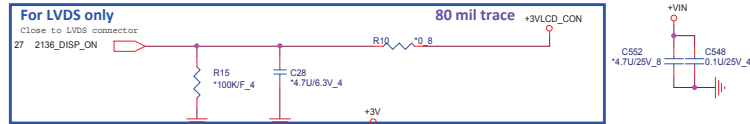
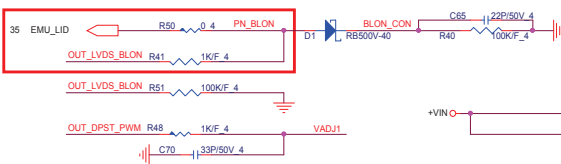
Document Number 27 - RTD2136

Date: Wednesday, May 06, 2015

Rev 1A

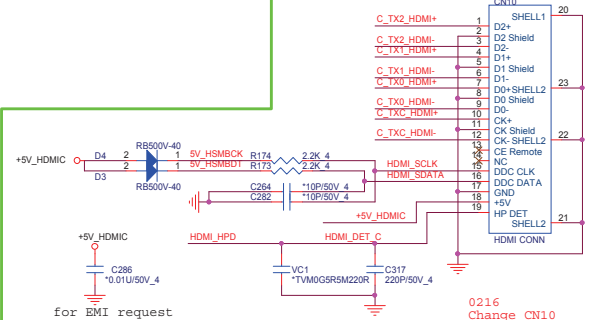
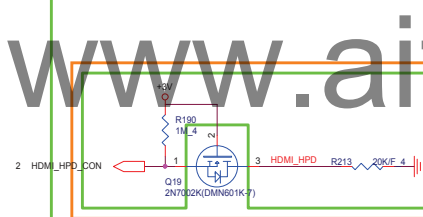
Sheet 27 of 49

LID Switch

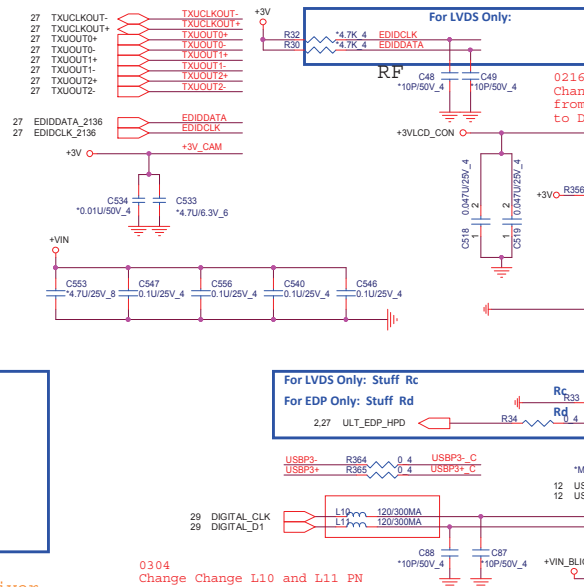
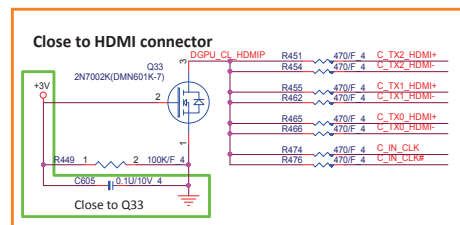
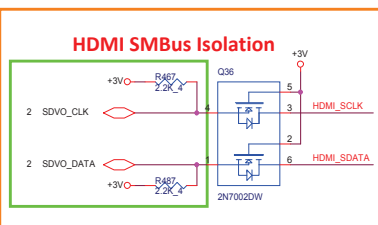


Without Re-driver

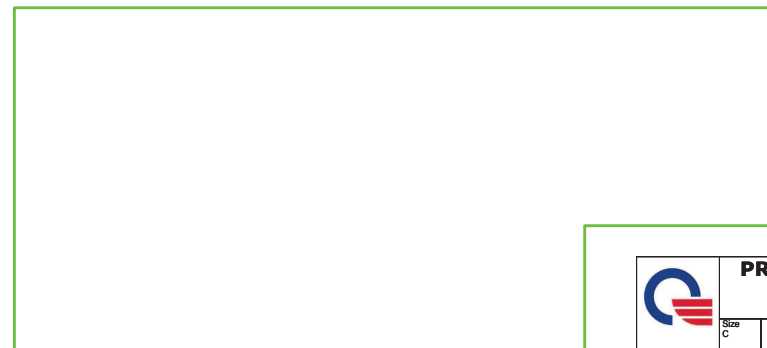
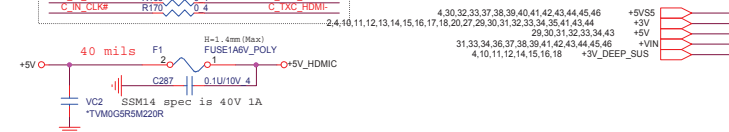
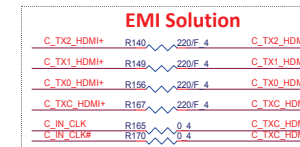
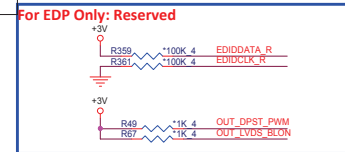
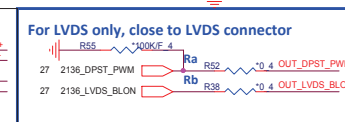
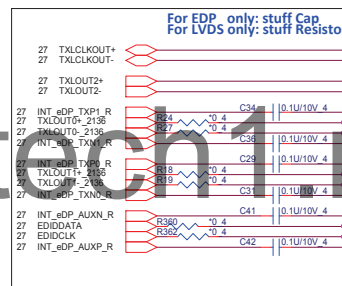
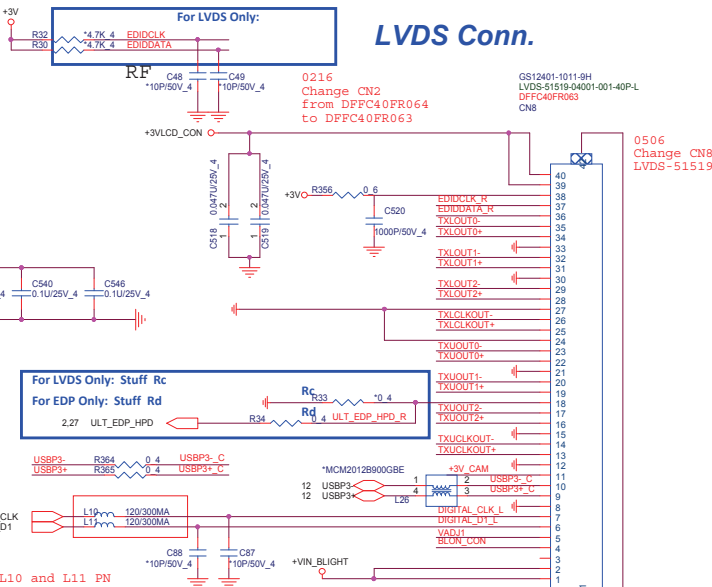
Re-driver



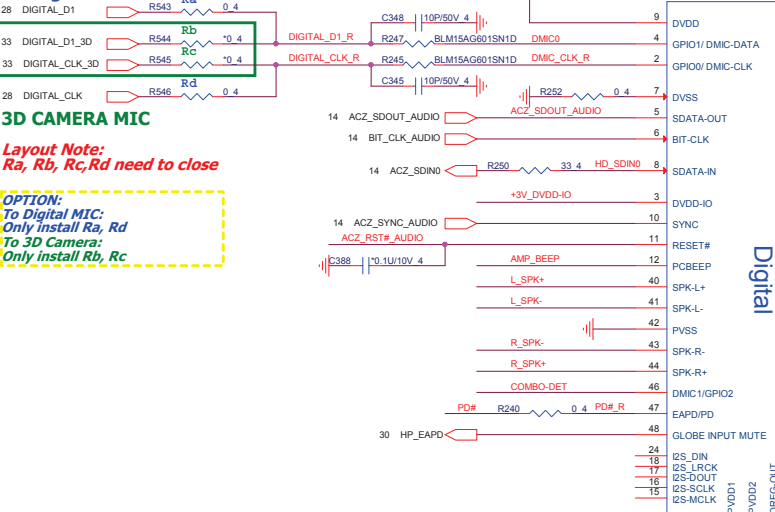
0216
Change CN10
from DFHD19MR249
to DFHD19MR422



0304
Change Change L10 and L11 PM

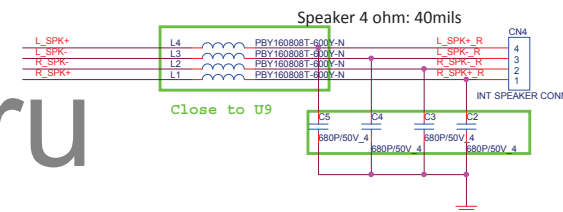
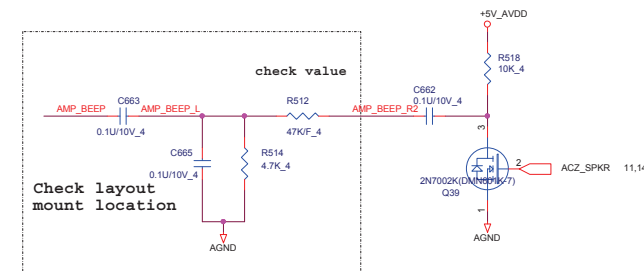
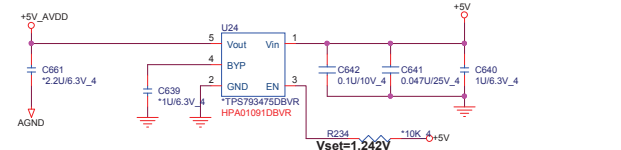
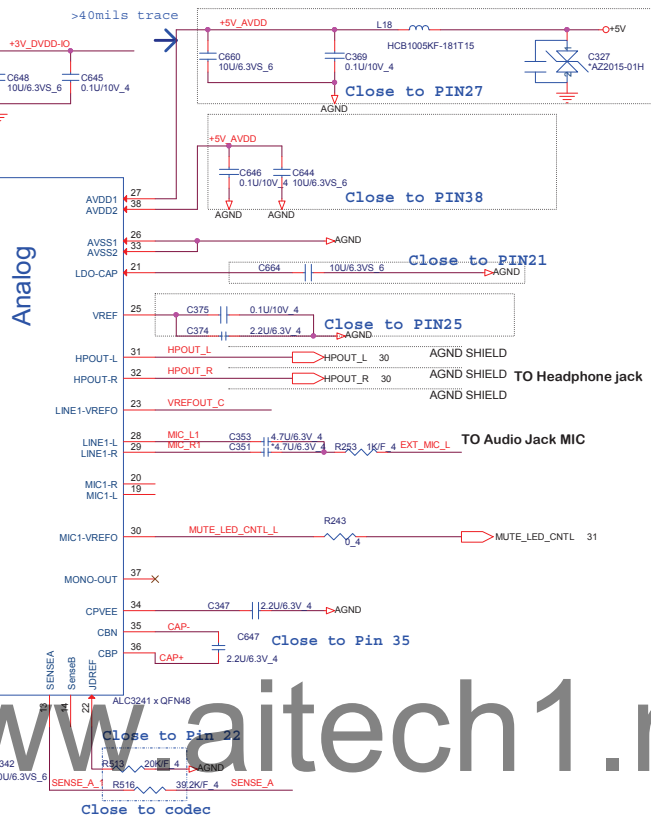
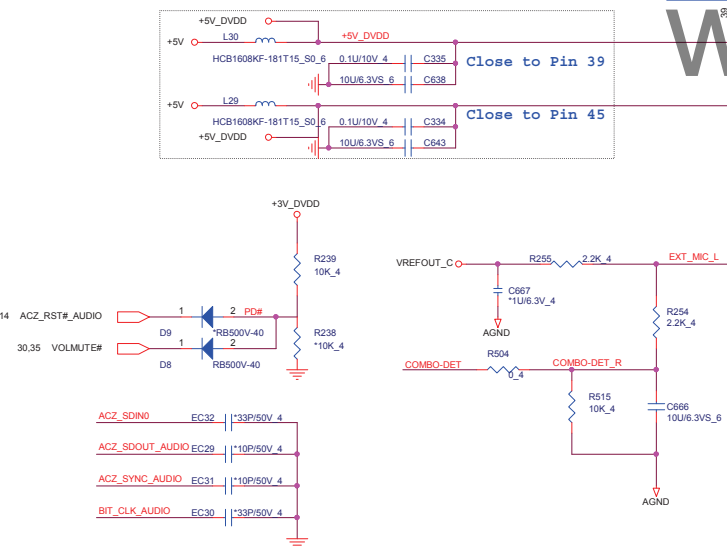


TO Digital MIC

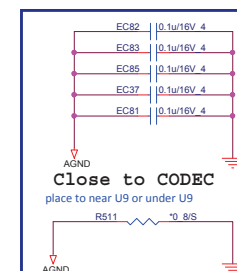


Layout Note:
Ra, Rb, Rc, Rd need to close

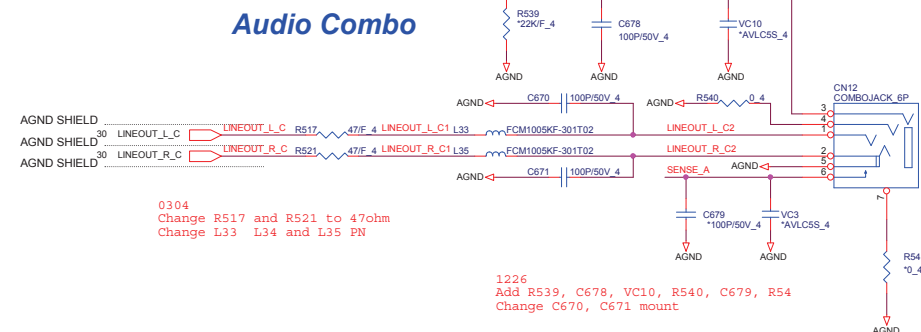
OPTION:
To Digital MIC:
Only install Ra, Rd
To 3D Camera:
Only install Rb, Rc



0306
Change EC37, EC81, EC82, EC83
EC85 from 1000P to 0.1u

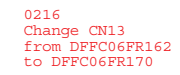


2,4,10,11,12,13,14,15,16,17,18,20,27,28,30,31,32,33,34,35,41,43,44 +3V
28 30 31 32 33 34 43 +5V



0304
Change R517 and R521 to 47ohm
Change L33 L34 and L35 PN

1226
Add R539, C678, VC10, R540, C679, R541
Change C670, C671 mount



KEYBOARD Con.

35 MY[0..17] → MY[0..17]
35 MX[0..7] → MX[0..7]

29 MUTE_LED_CNTL → MUTE_LED_CNTL_R1

Q26 2N7002K(DMN601K-7)

R348 10K_4

35 CAPSLED# → MUTE_LED_CNTL_R1

R341 2 R342 2 1 200/F 6 CAPSLED# R MUTE_LED_CNTL_R WIRELESS_ON_R WIRELESS_OFF_R LED_PW

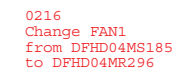
+3V0

KB1
51586-03241-001-32p-I
DFFC32FR043
KB 14" & 15"

KB2
51586-03241-001-32p-I
DFFC32FR043
KB 17"

0216 Change KB1/KB2 from DFFC32FR042 to DFFC32FR043

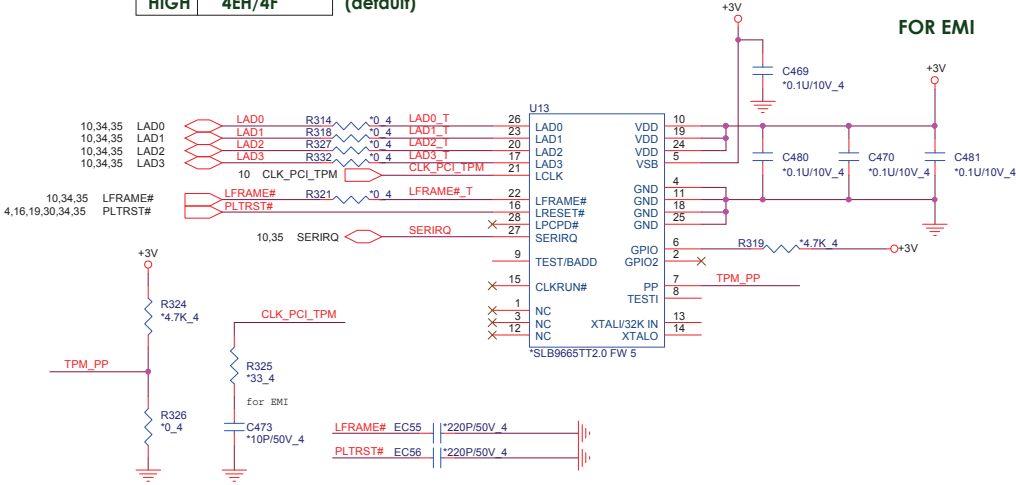
www.aitec.com



TPM (2.0)

Address

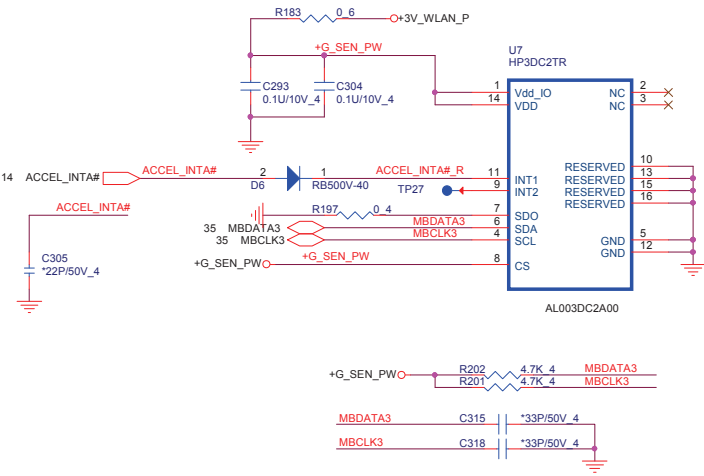
	BADD
HIGH	4EH/4F (default)



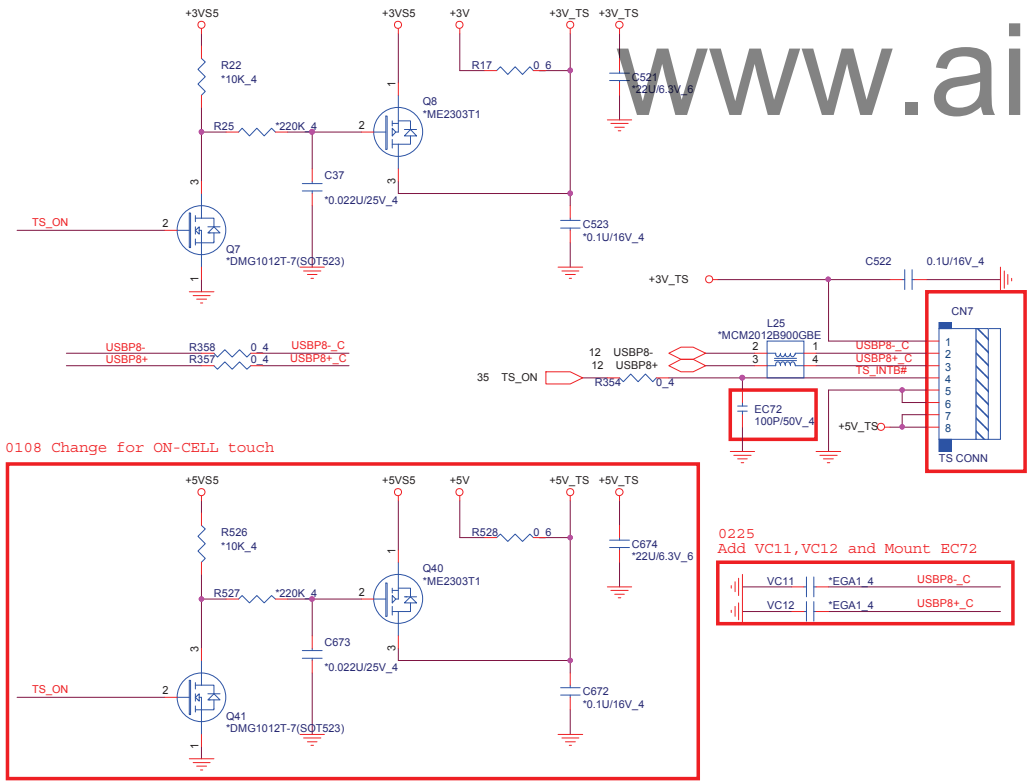
Accelerometer Sensor

32

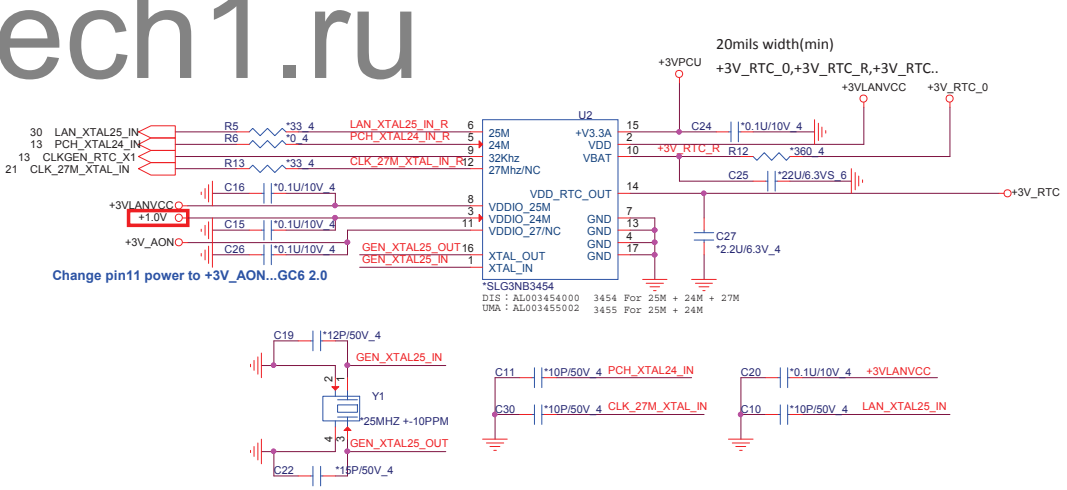
G-Sensor Power need check



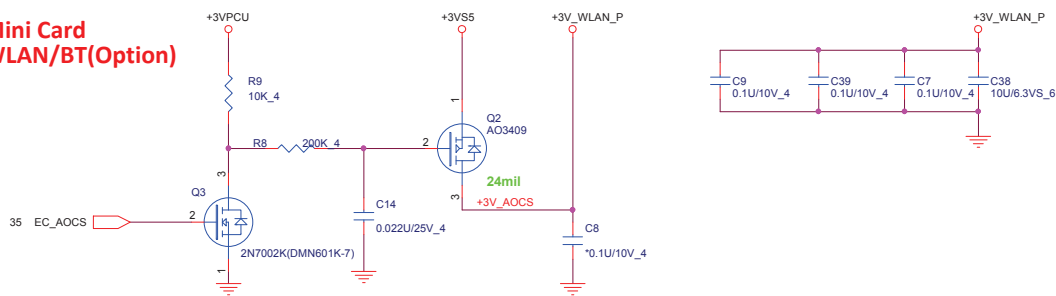
Touch screen



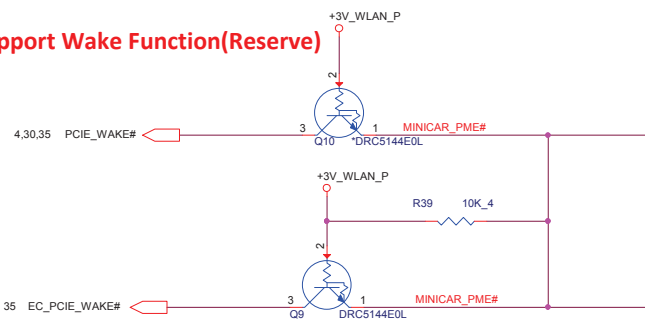
Green CLK Circuitry



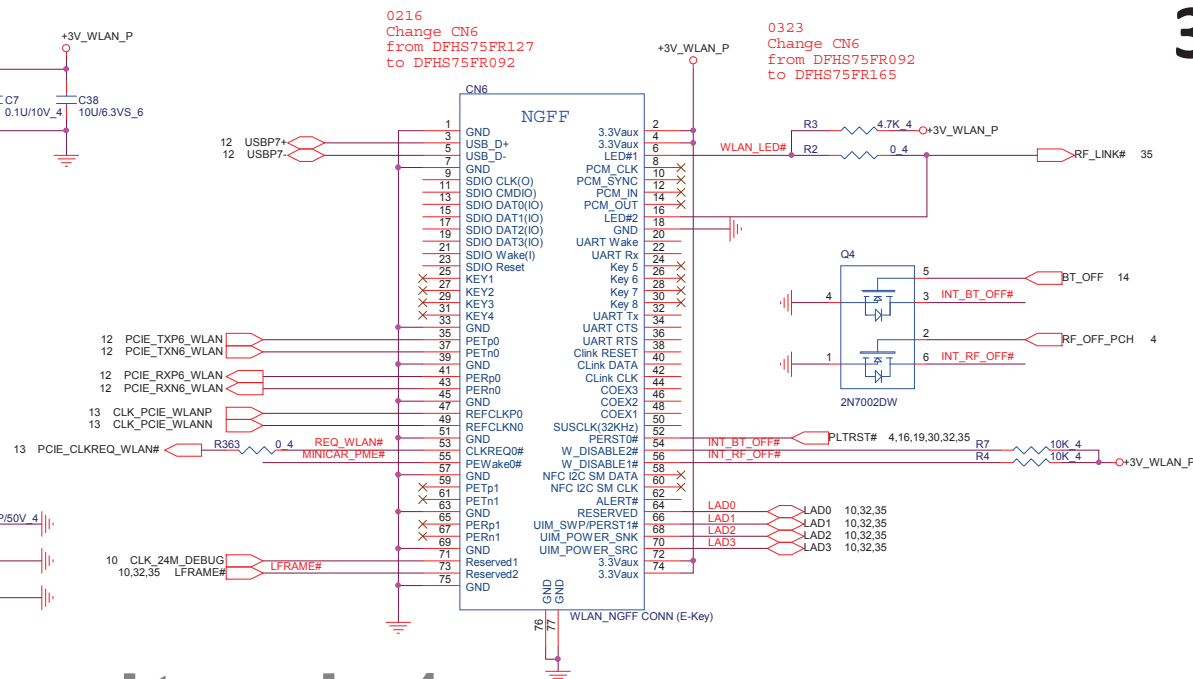
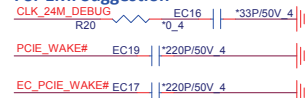
Mini Card WLAN/BT(Optional)



Support Wake Function(Reserve)

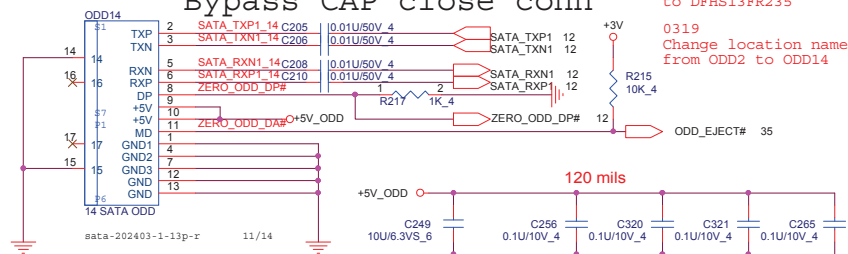


For EMI Suggestion

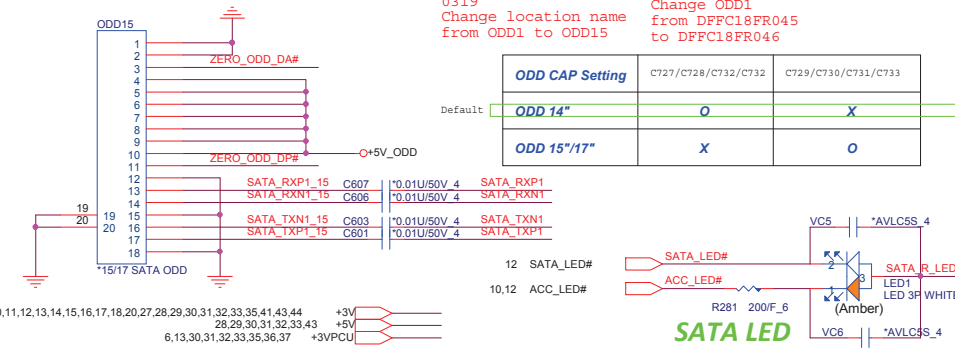


14" SATA ODD

Bypass CAP close conn



15/17 " SATA ODD

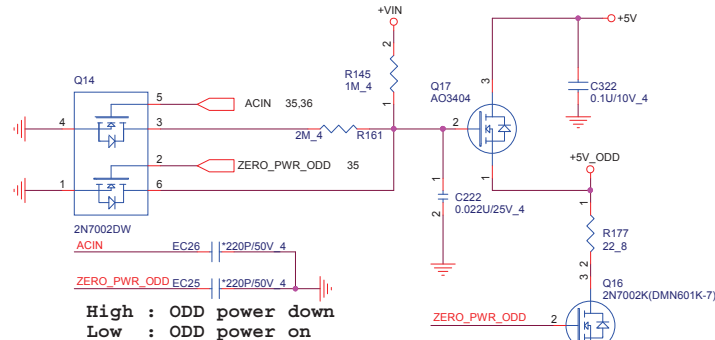


0216
Change ODD2
from DFHS13FR035
to DFHS13FR235

0319
Change location name
from ODD2 to ODD14

0319
Change location name
from ODD1 to ODD15

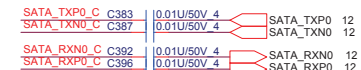
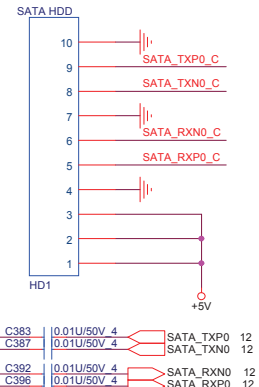
0216
Change ODD1
from DFFC18FR045
to DFFC18FR046

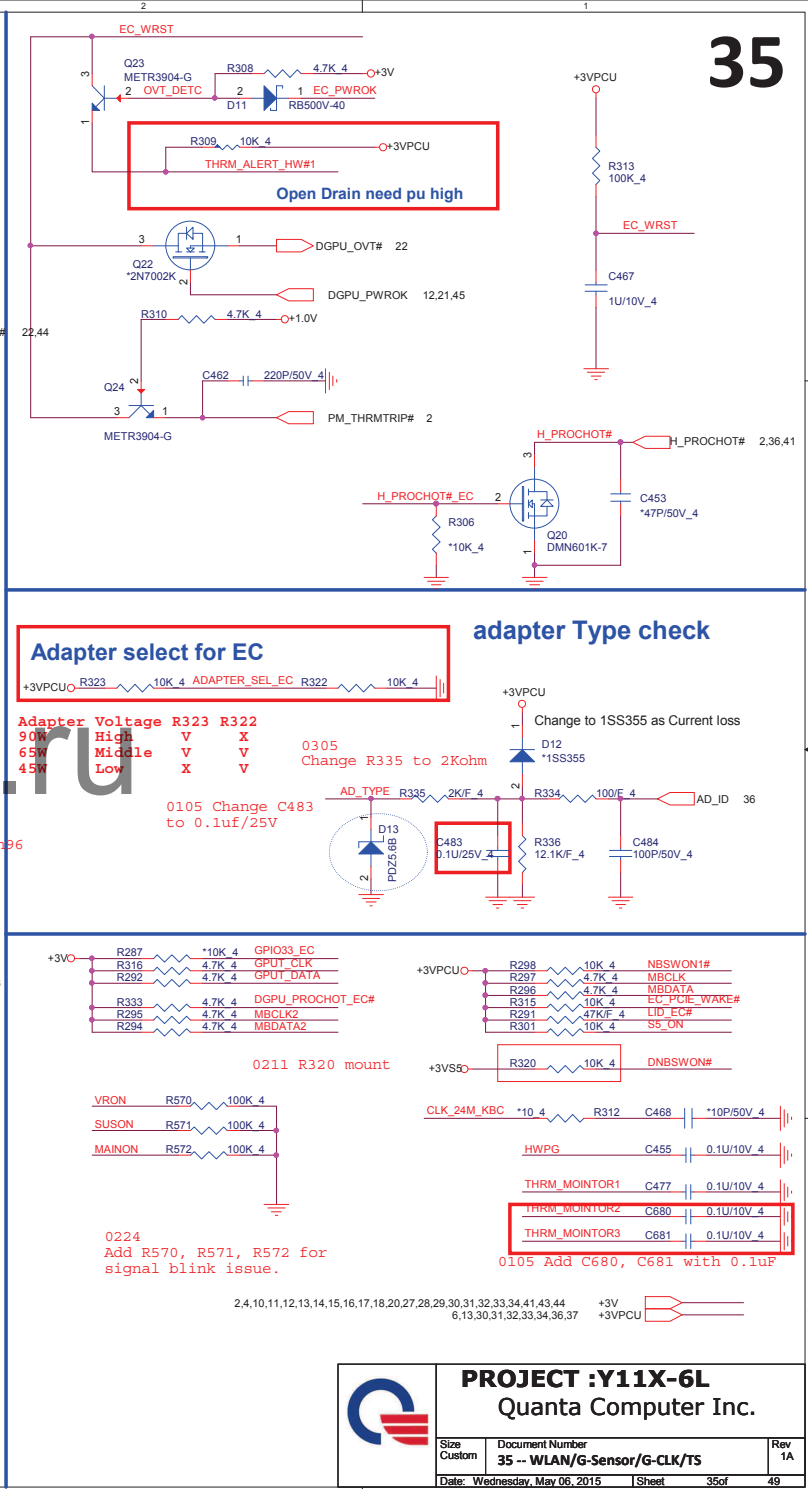
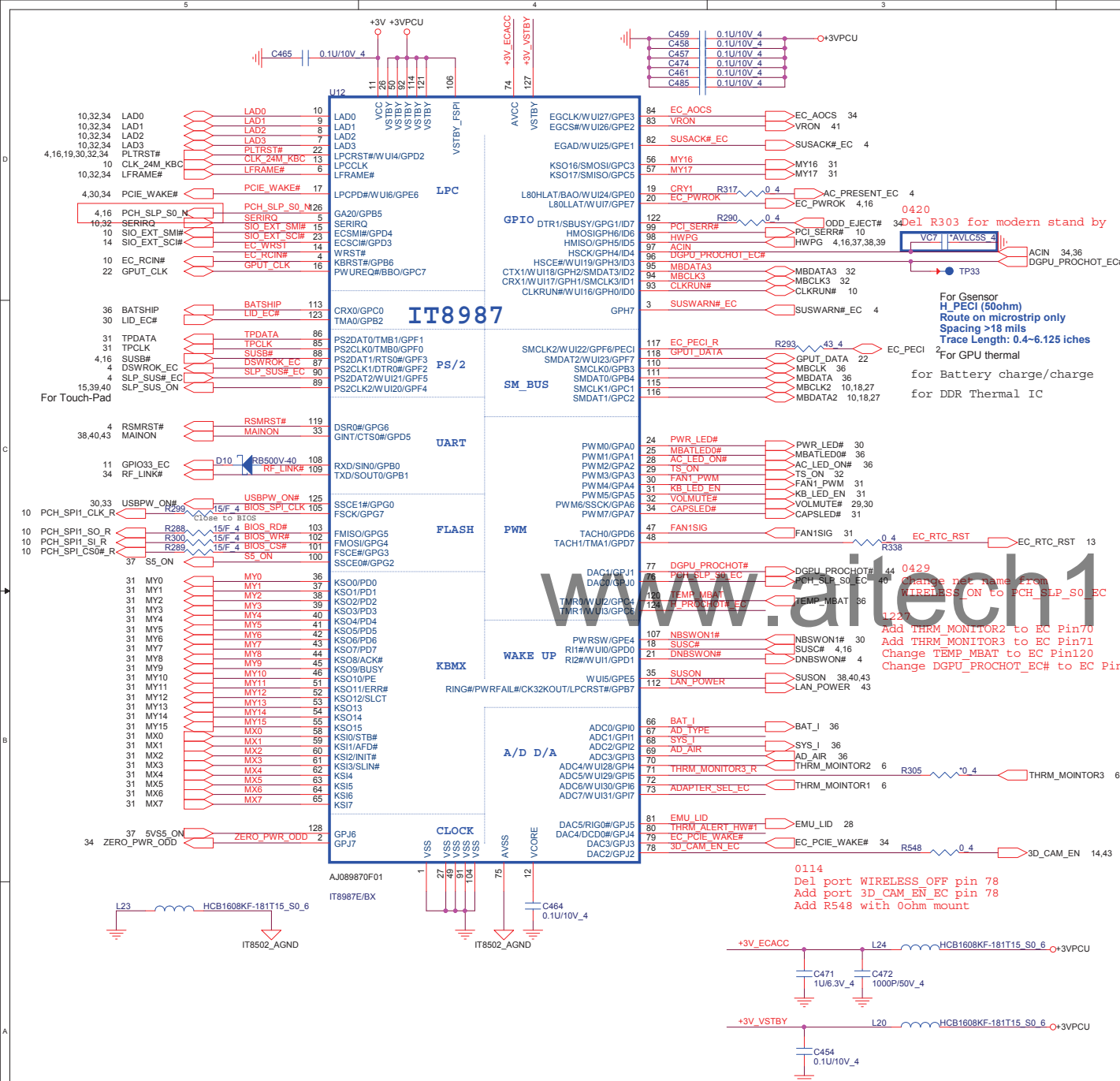


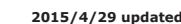
High : ODD power down
Low : ODD power on

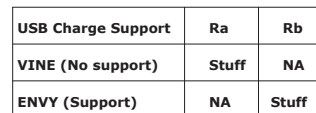
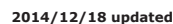
HDD

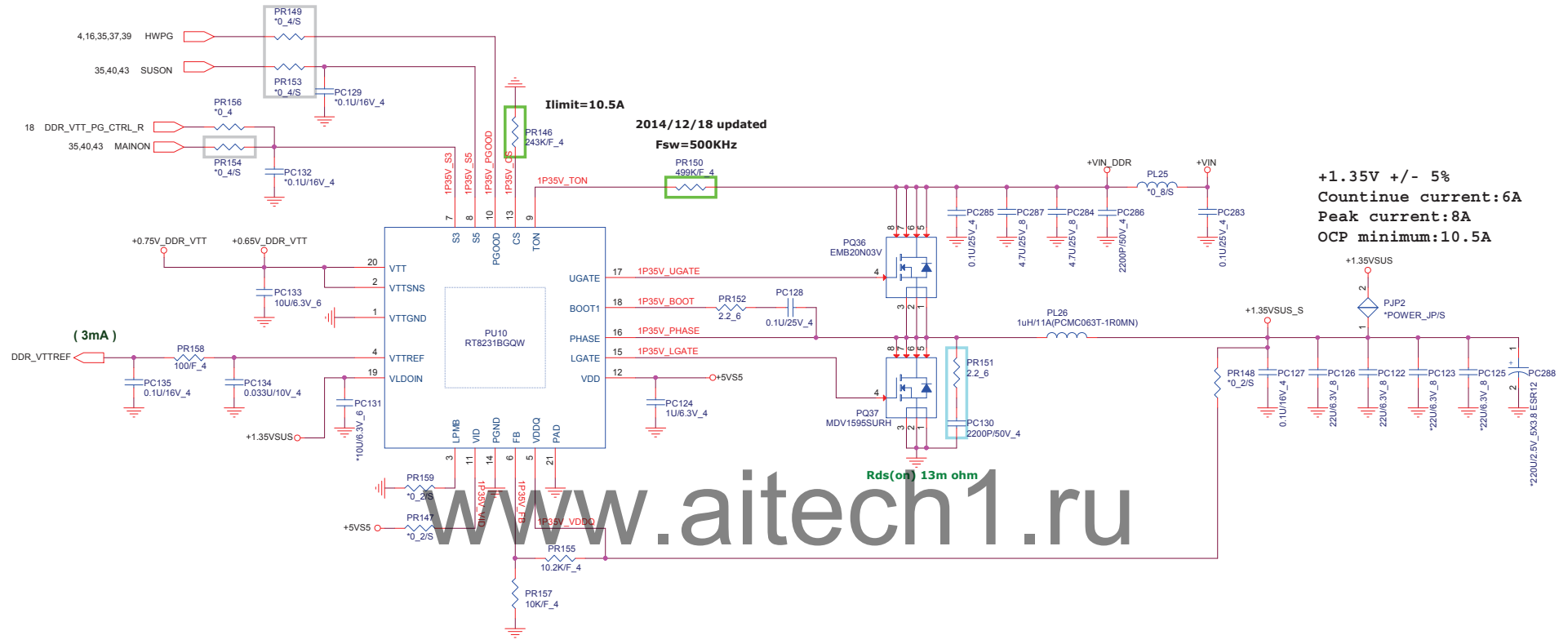
0216
Change HD1
from DFFC10FR113
to DFFC10FR112





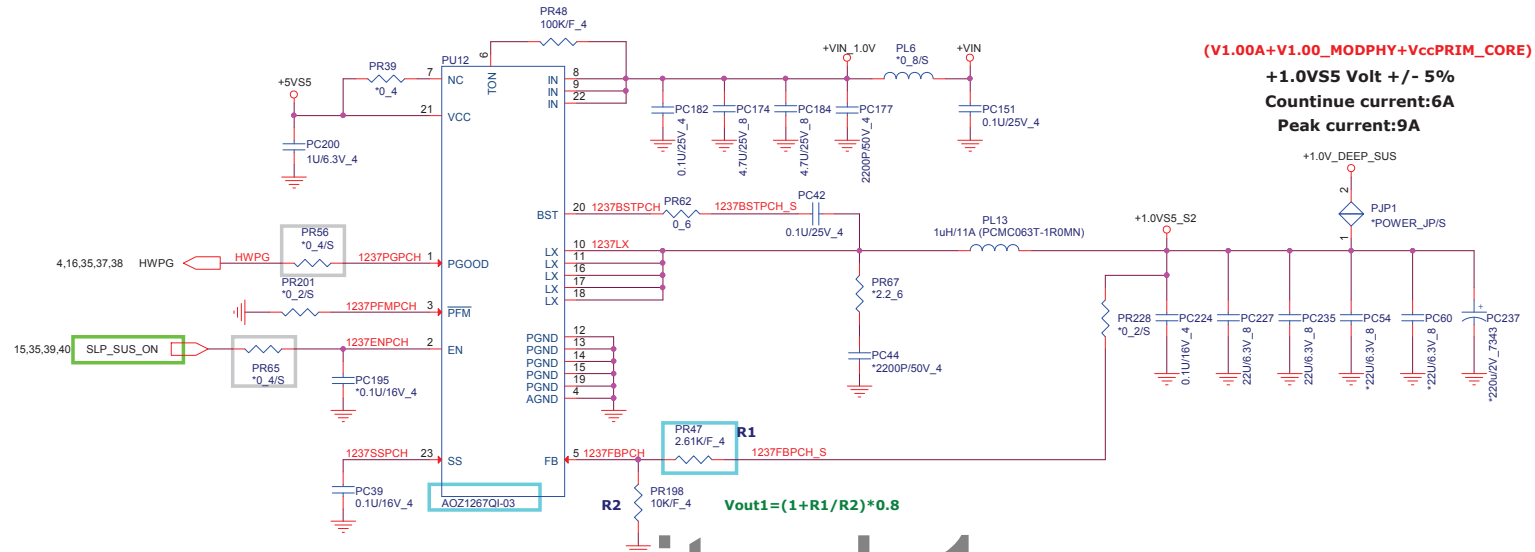




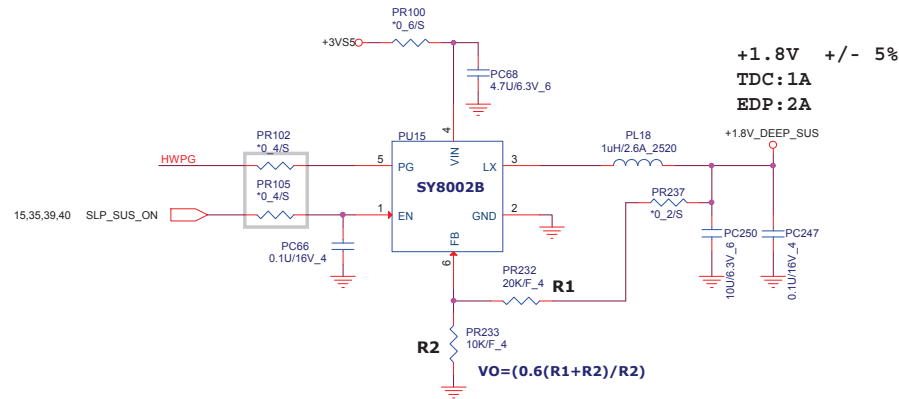


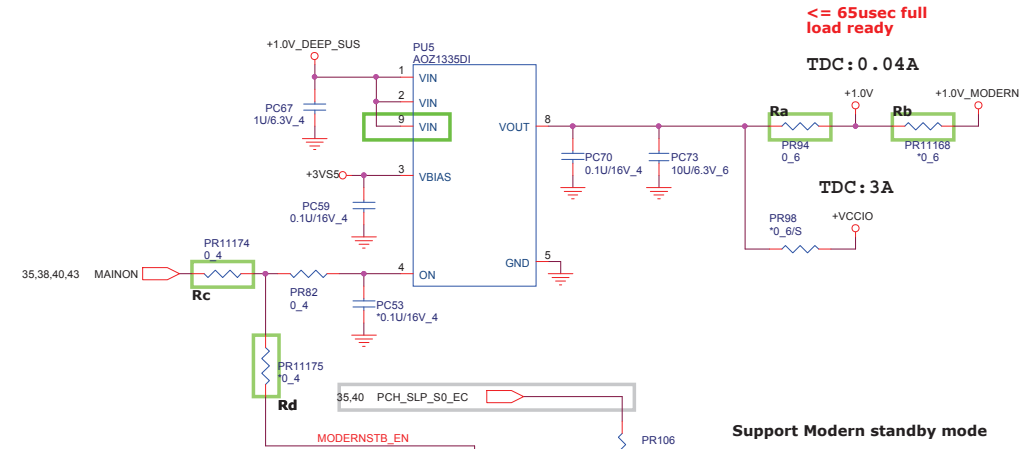
+VIN	28,31,33,34,36,37,39,41,42,43,44,45,46
+5VS5	4,30,32,33,37,39,40,41,42,43,44,45,46
+0.65V_DDR_VTT	17,18
+1.35VSUS	3,6,17,18,40,46

- +VIN 28,31,33,34,36,37,38,41,42,43,44,45,46
- +5VS5 4,30,32,33,37,38,40,41,42,43,44,45,46
- +3VS5 4,10,15,16,32,34,35,37,40,43,46
- +1.8V_DEEP_SUS 9,15
- +1.0V_DEEP_SUS 9,13,15,16,40

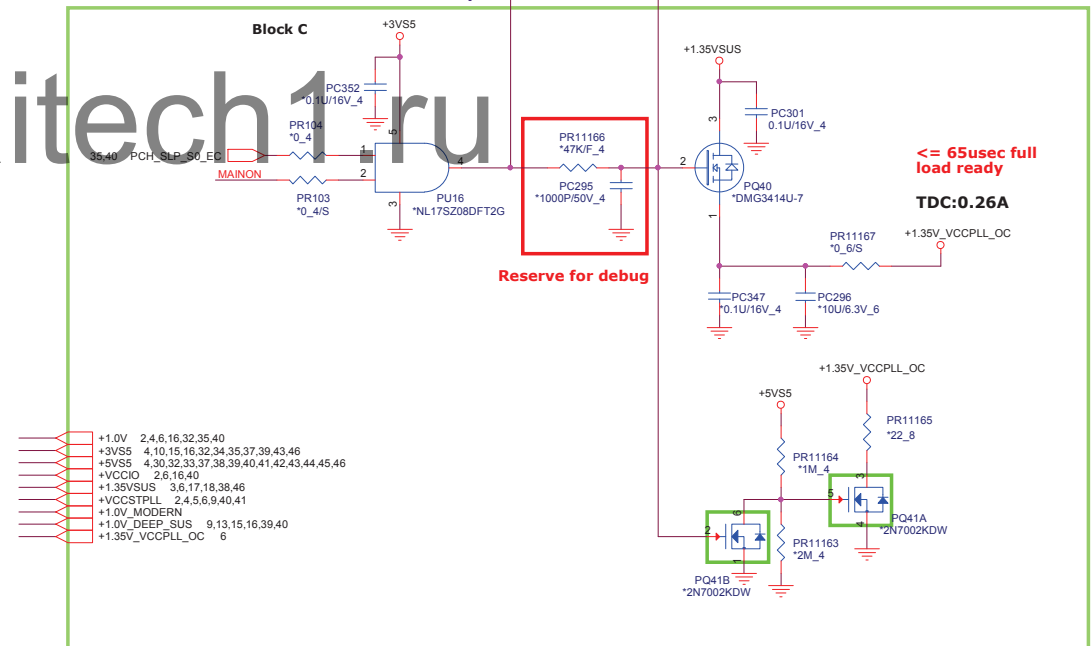
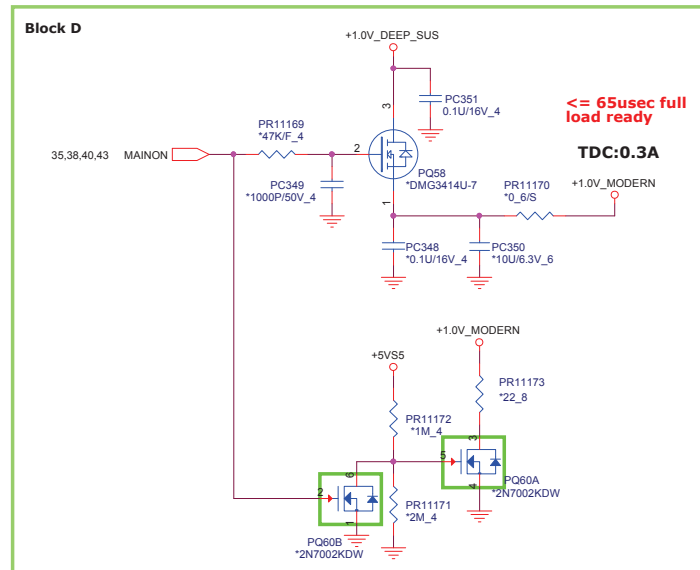


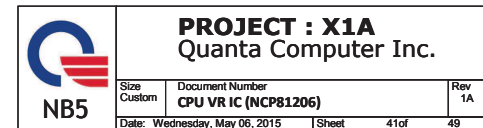
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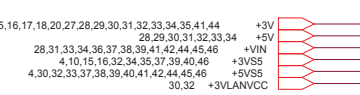


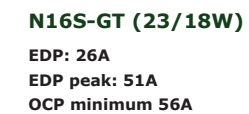


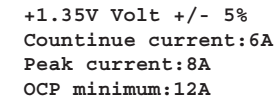
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